

Detector development at BNL



Gabriella Carini, D. Peter Siddons
National Synchrotron Light Source
Brookhaven National Laboratory
USA

Outline

- BNL projects
 - ☒ Spectroscopy
 - ☒ Germanium
 - ☒ Imaging
 - ☒ Future
- Summary



The ideal detector

- Should have:

-  10^9 pixels

-  1 μm spatial resolution

-  1 eV energy resolution

-  1 fs time resolution

-  count rates up to 10^9 / pixel

-  Efficient from 100 eV out to 100 keV

The ideal detector

- Should have:

- 10^9 pixels

- 1 μm spatial resolution

- 1 eV energy resolution

- 1 fs time resolution

- count rates up to 10^9 / pixel

- Efficient from 100 eV out to 100 keV

– **And it should be free!**

Required infrastructure for complete detector development

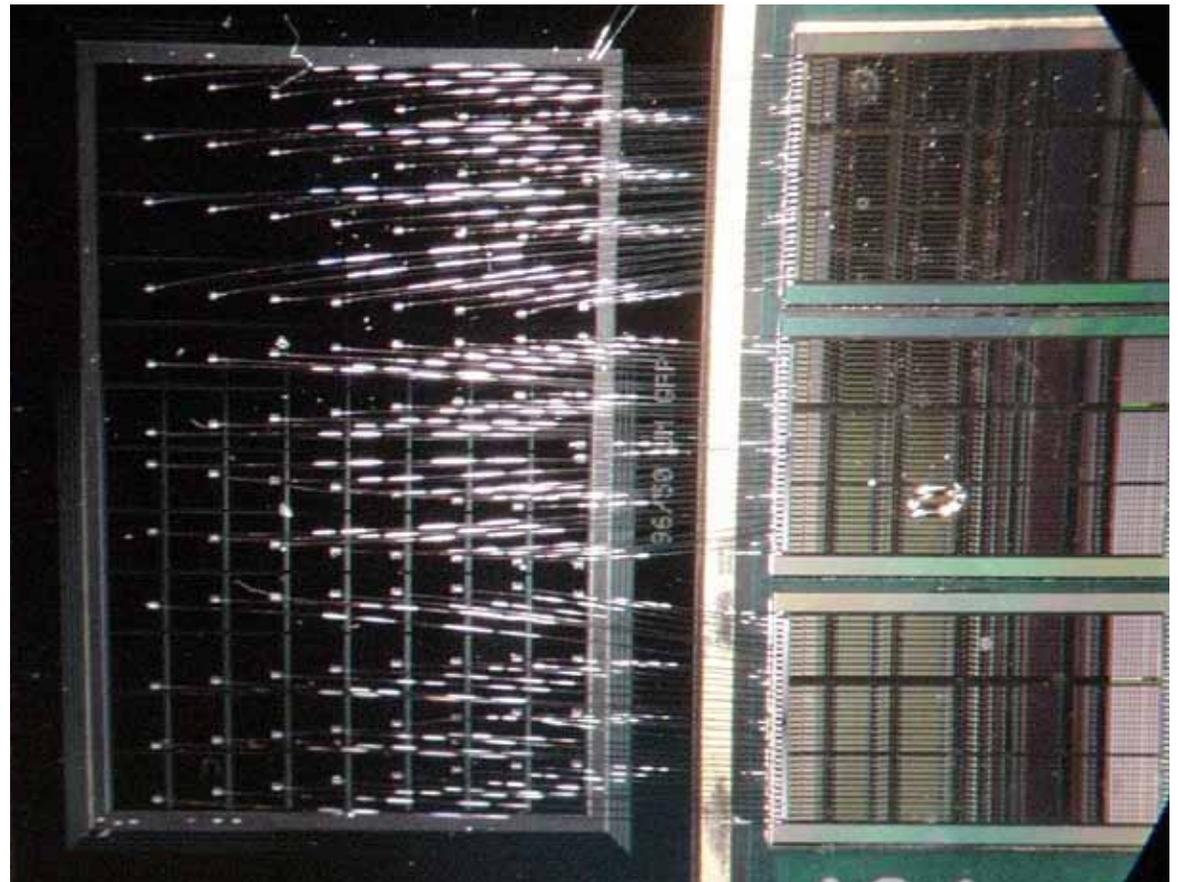
- Expertise in semiconductor science and access to software tools to enable the development of new types of sensor
- A specialized foundry to make these devices
- Expertise in the design and fabrication of custom microcircuits and access to state-of-the-art design tools
- Expertise in conventional electronics, both analog and digital
- Expertise in data acquisition and system integration.

Outline

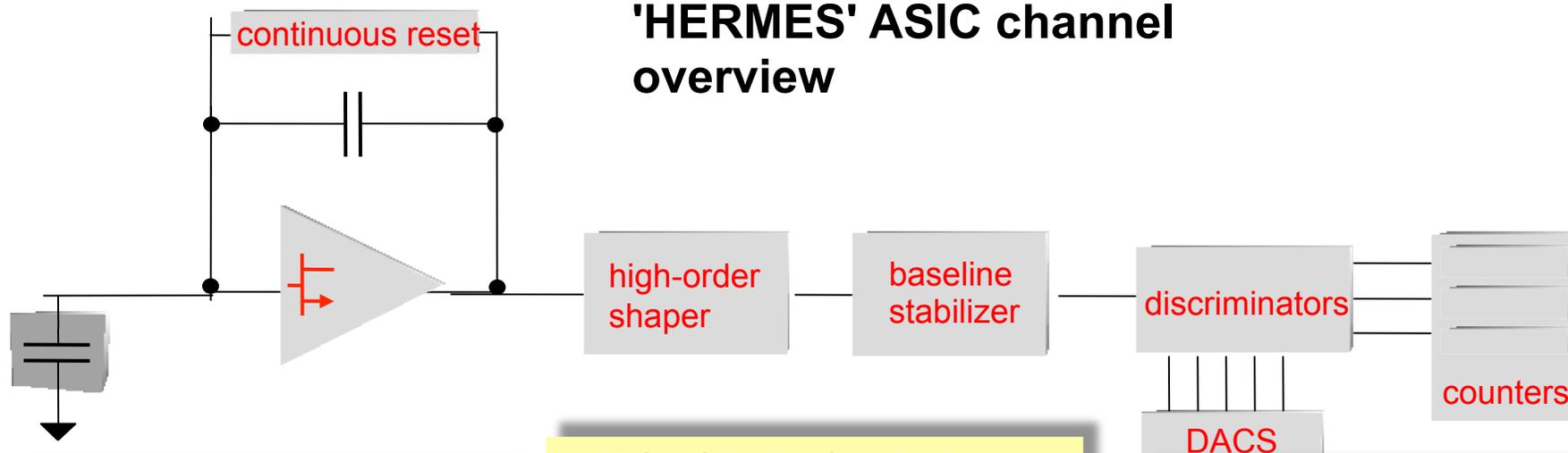
- BNL Projects
 - ☒ Spectroscopy
 - ☒ Germanium
 - ☒ Imaging
 - ☒ Future
- Summary

Maia X-ray Fluorescence Microprobe detector

- 96 pads, 1mm x 1mm, wire-bonded to 3 ASICs.
- The long bonds are rather fragile, but this approach provided least parasitic capacitance.
- Each ASIC provides 32 channels of low-noise analog/digital processing.
- ASIC appears to have 100% yield (no bad channels to date).



'HERMES' ASIC channel overview



INPUT p-MOSFET

- optimized for operating region
- NIM A480, p.713

CONTINUOUS RESET

- feedback MOSFET
- self adaptive 1pA - 100pA
- low noise < 3.5e⁻ rms @ 1μs
- highly linear < 0.2% FS
- US patent 5,793,254
- NIM A421, p.322
- TNS 47, p.1458

☒ 3 mW

HIGH ORDER SHAPER

- amplifier with passive feedback
- 5th order complex semigaussian
- 2.6x better resolution vs 2nd order
- TNS 47, p.1857

BASELINE STABILIZER (BLH)

- low-frequency feedback, BGR
- slew-rate limited follower
- DC and high-rate stabilization
- dispersion < 3mV rms
- stability < 2mV rms @ rt ☒ tp < 0.1
- TNS 47, p.818

☒ 5 mW

DISCRIMINATORS

- five comparators
- 1 threshold + 2 windows
- four 6-bit DACs (1.6mV step)
- dispersion (adj) < 2.5e⁻ rms
- five 10-bit DACs
- reference voltages for comparators

COUNTERS

- three (one per discriminator)
- 24-bit each

ASIC

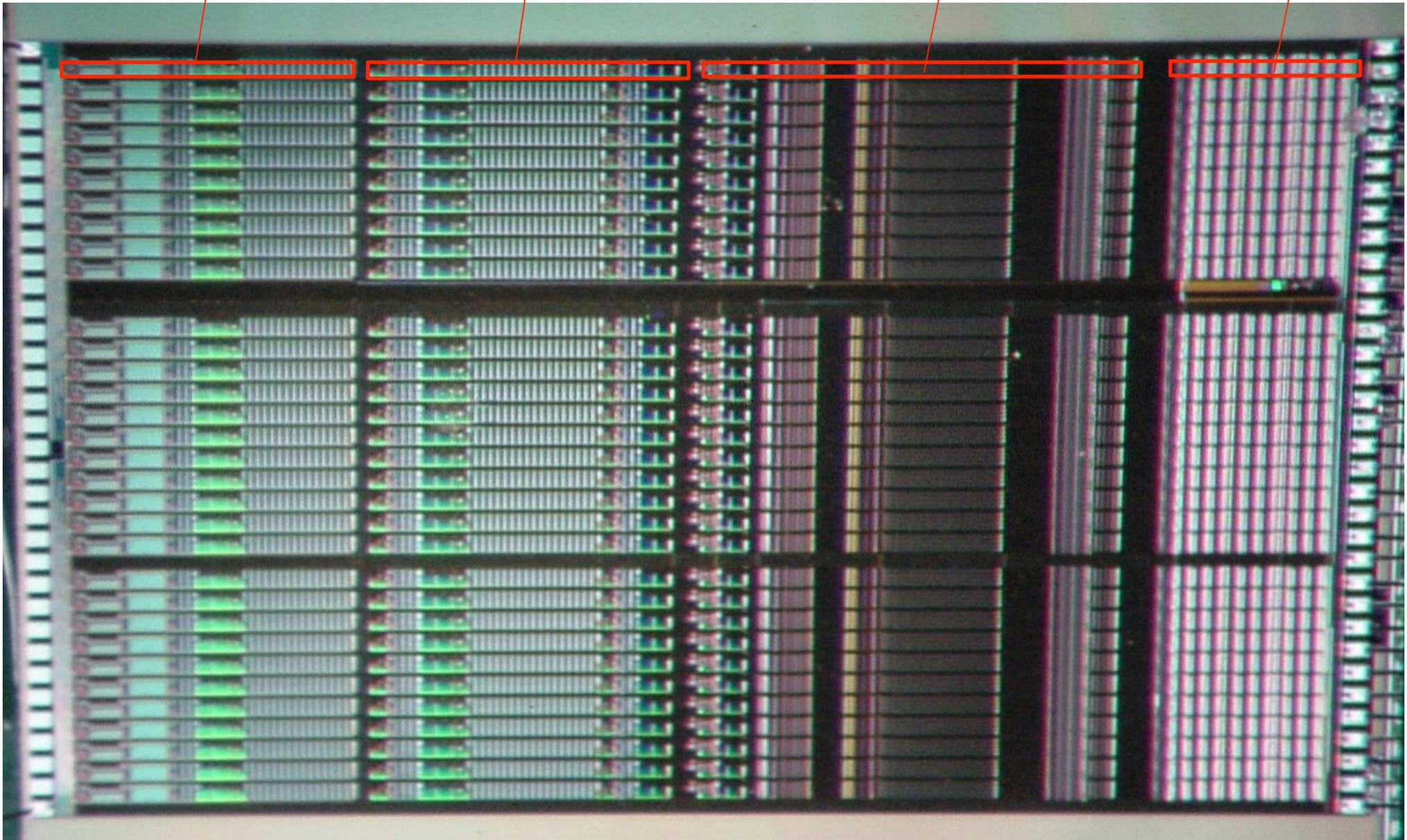
'HERMES' ASIC photo

charge preamplifier

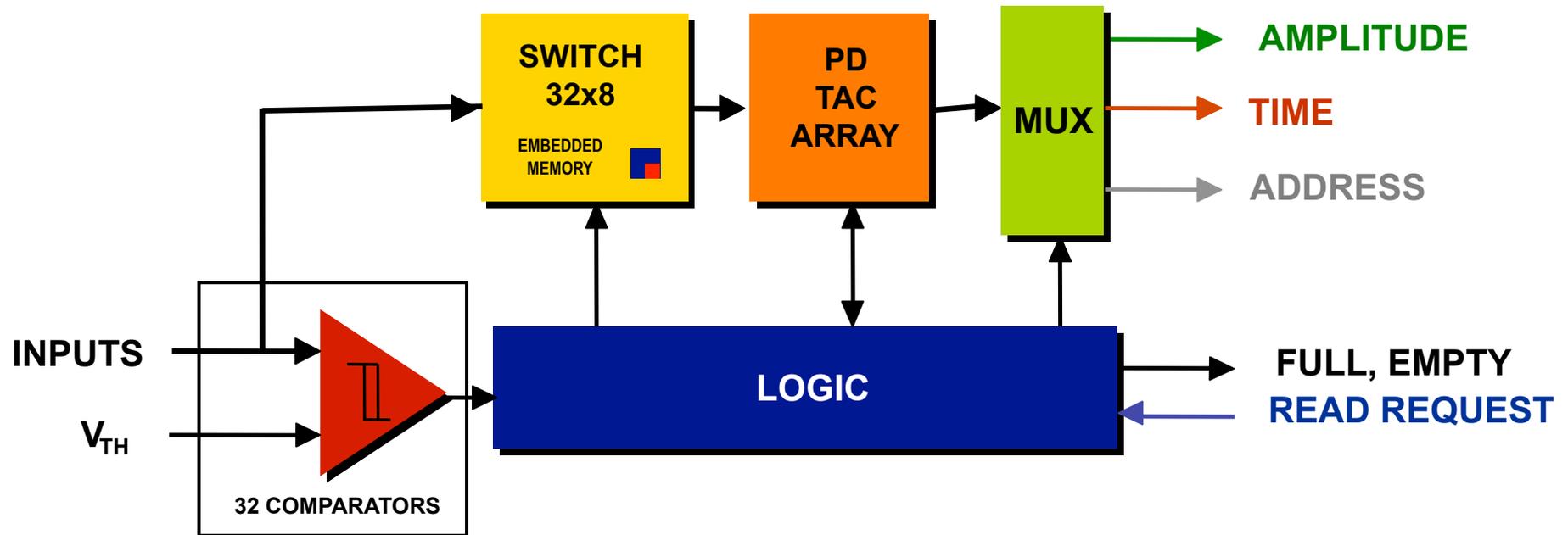
shaper with BLH

discriminators and DACs

counters



The Peak Detector Derandomizer ASIC Architecture



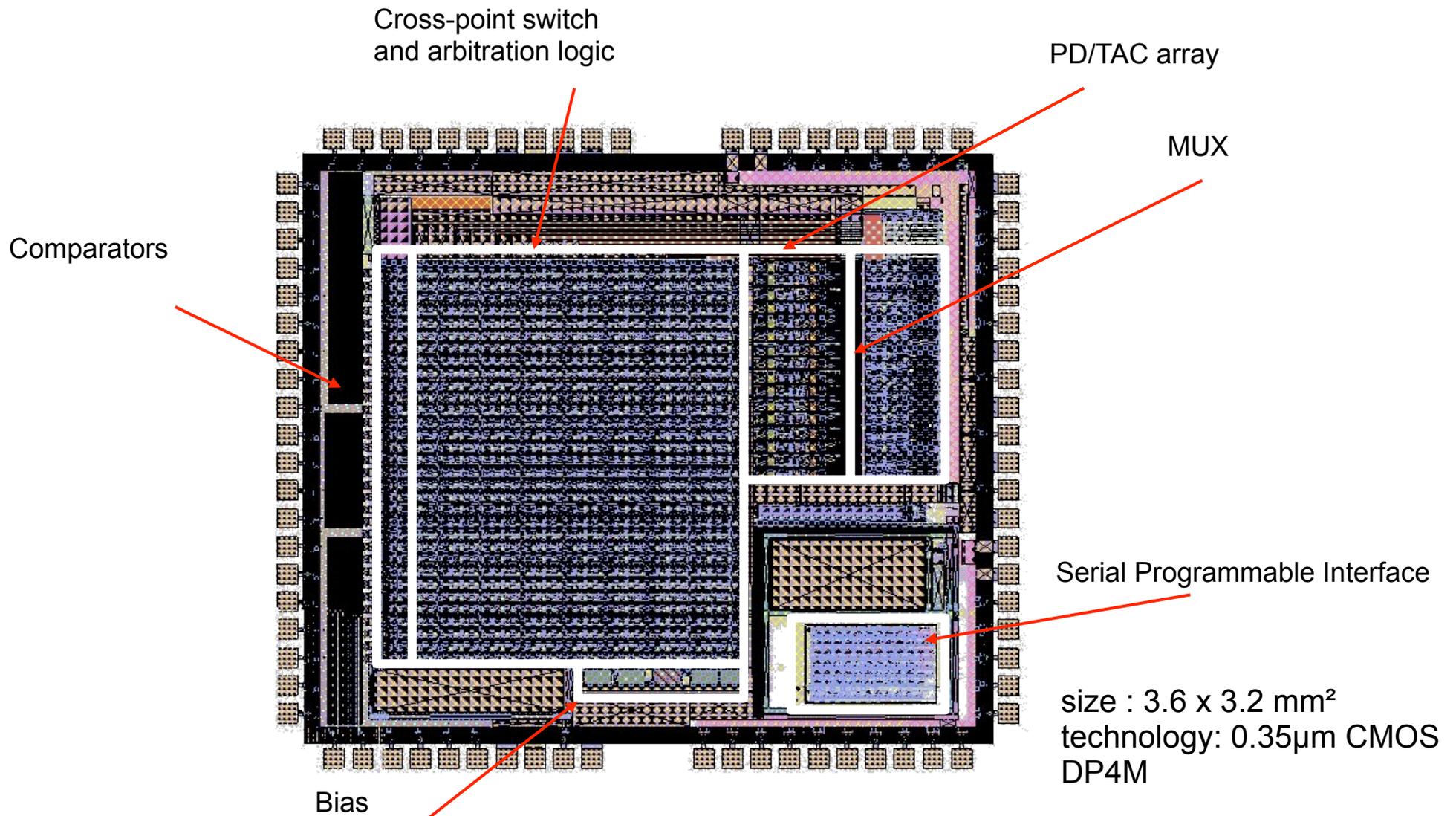
New architecture for efficient readout of multichannel detectors

- *Self-triggered and self-sparsifying*
- *Simultaneous amplitude, time, and address measurement for 32 input channels*
- *Set of 8 peak detectors act as derandomizing analog memory*
- *Rate capability improvement over present architectures*

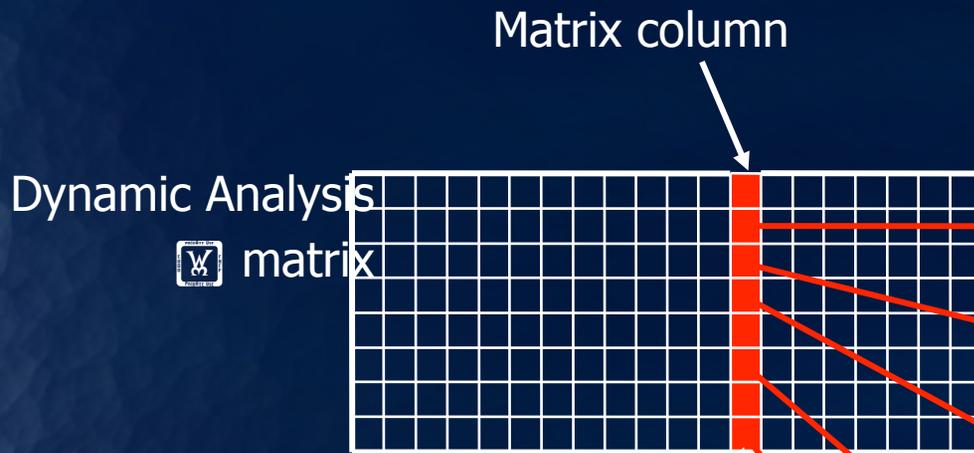
Based on new 2-phase peak detector combined with Quad-mode TAC

- *High absolute accuracy (0.2%) and linearity (0.05%), timing accuracy (5 ns)*
- *Accepts pulses down to 30 ns peaking time, 1.6 MHz rate per channel*
- *Low power (2 mW per channel)*

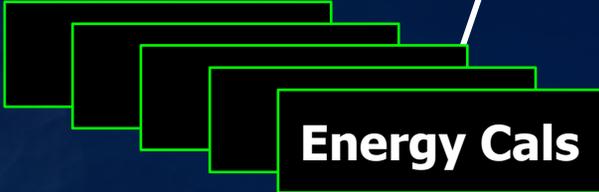
Scepter Layout



Real-time Elemental Imaging ...



N:



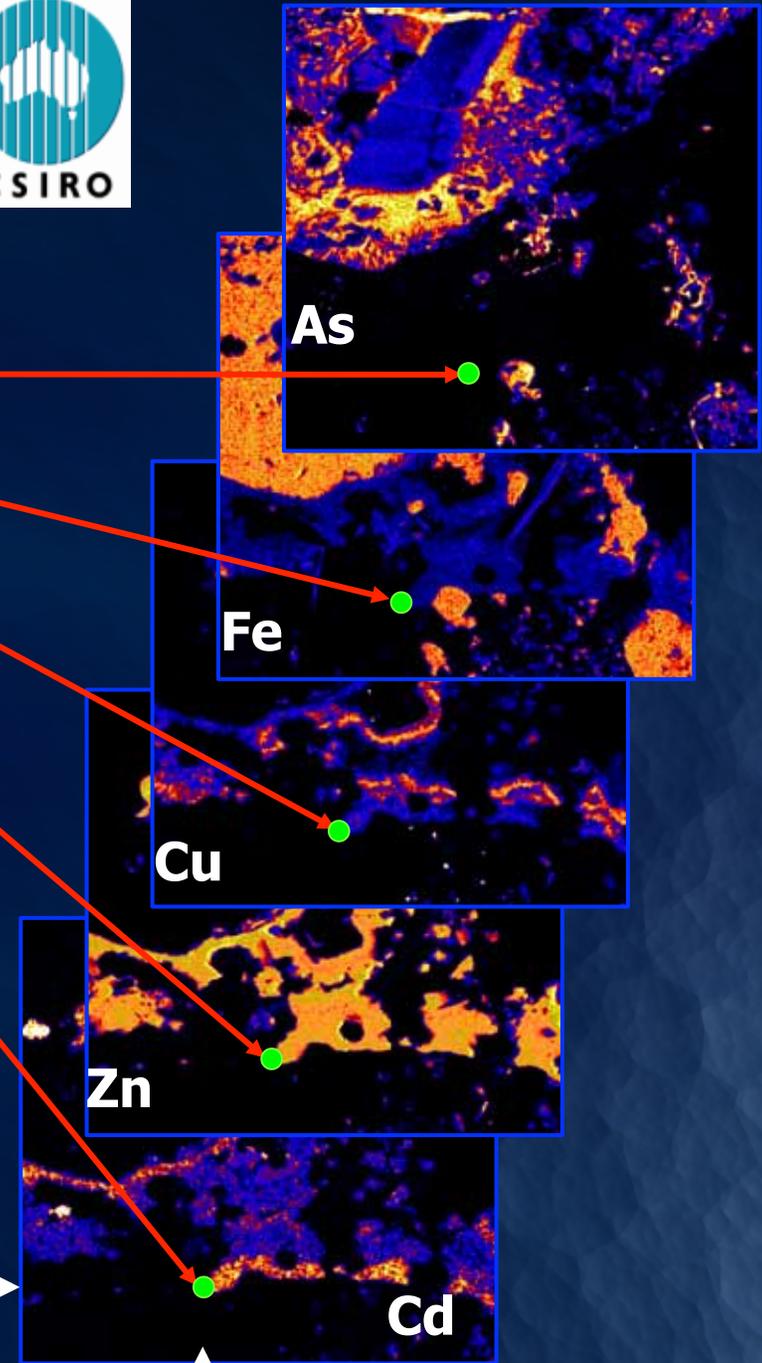
Energy Cals

Event: Detector **N**, Channel **i(E)**, Position **X,Y**



Detectors

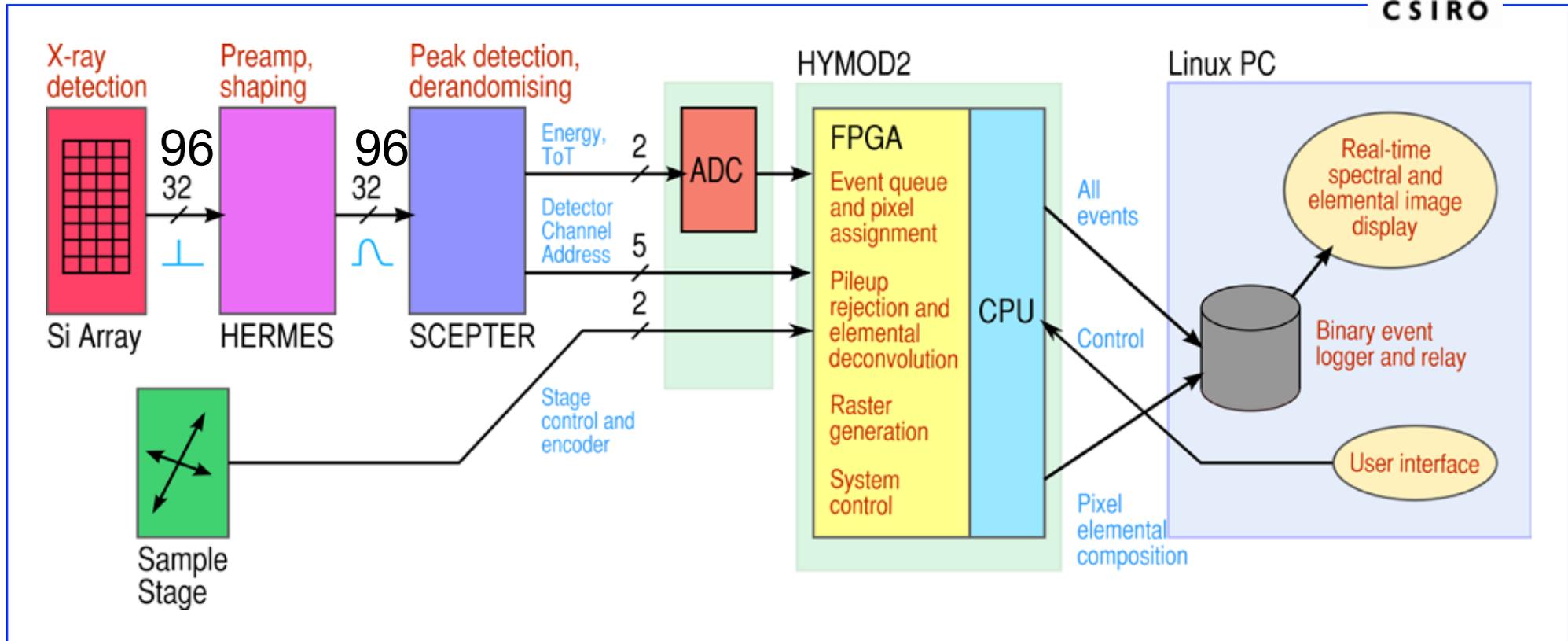
X



Y



Demonstration experiment at X27A: Block diagram of test setup



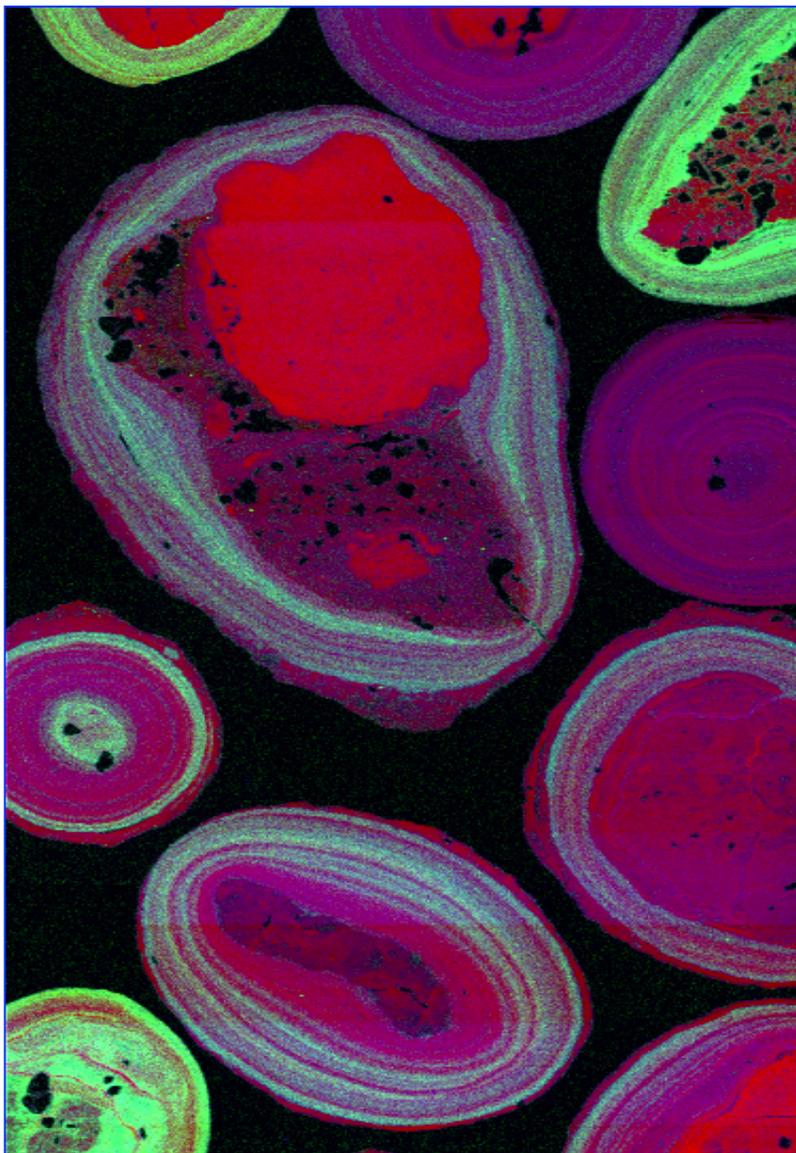
- HYMOD controls stage and reads detector
- Each photon tagged with energy, XY position and pileup status
- Initial coarse scan generates 'average' spectrum which makes DA matrix
- DA technique then presents elemental map as acquisition proceeds.



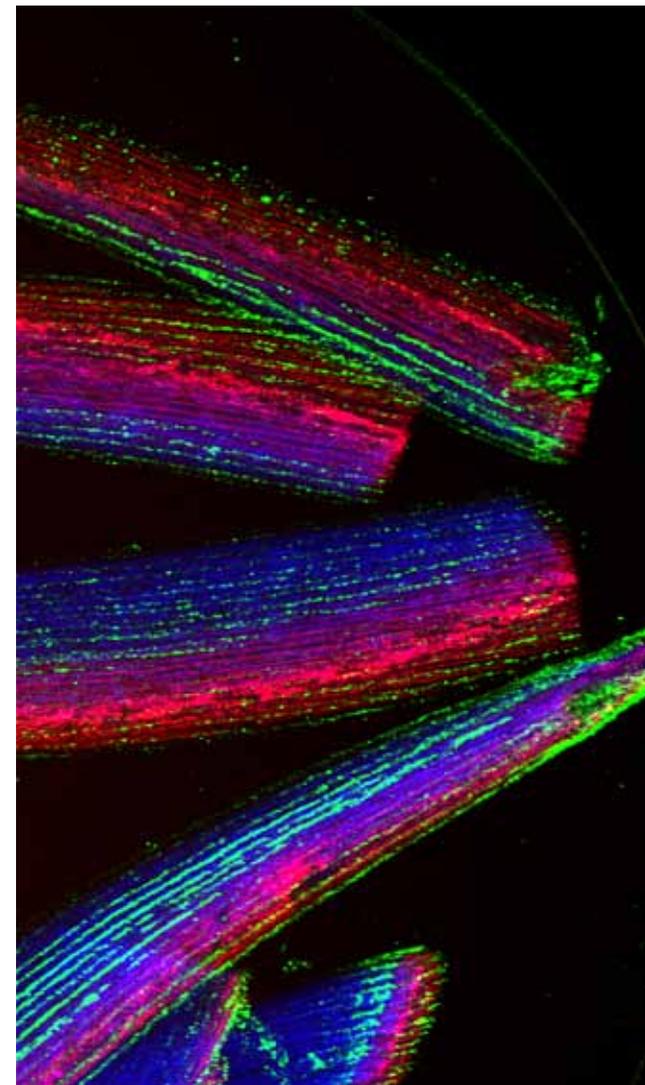
Rapid XRF Elemental Mapping (BNL/CSIRO collaboration)



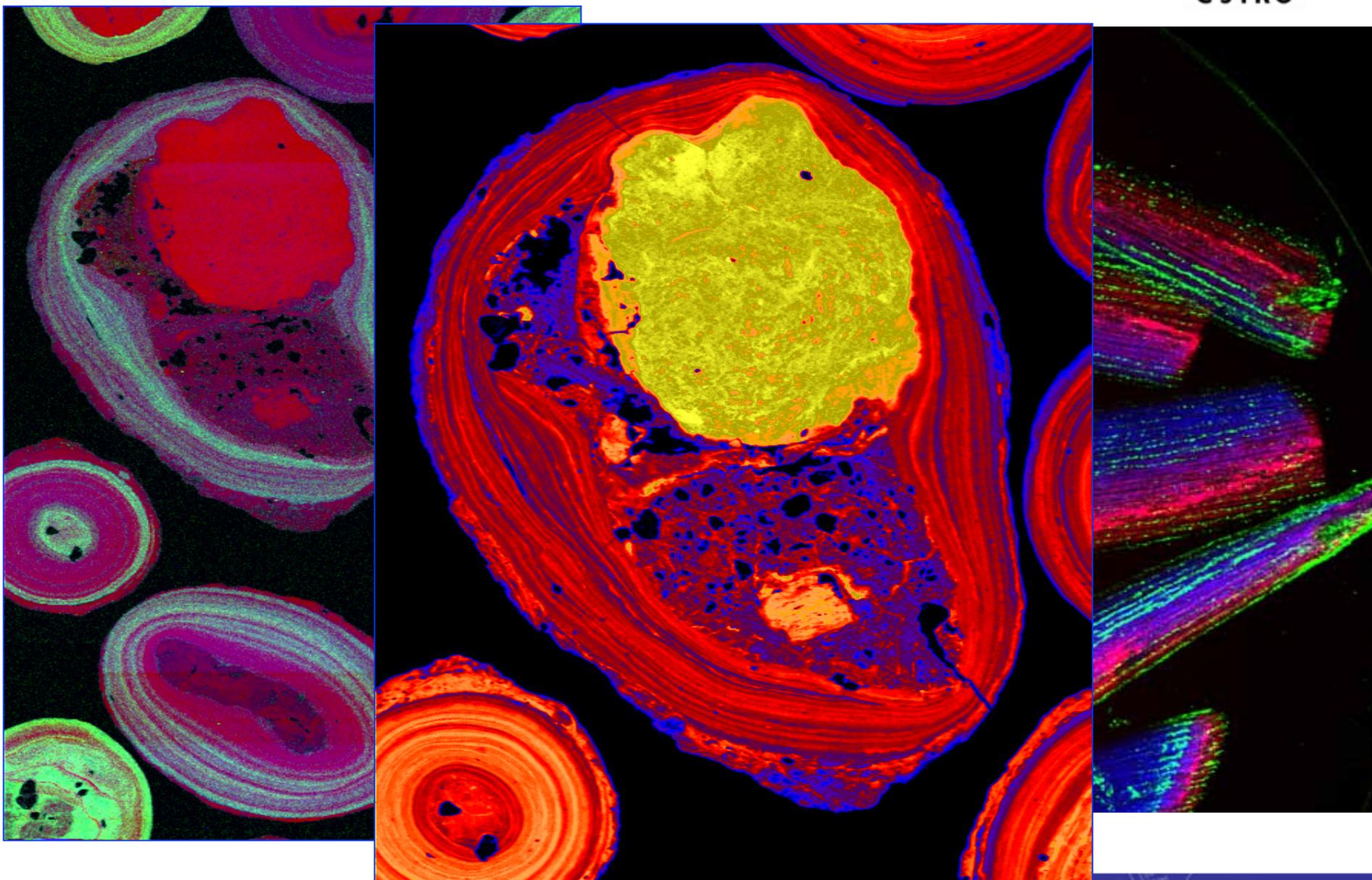
Fe-Y-Cu RGB composite (1500 x 2624 pixel images, 13 x 21 mm²)



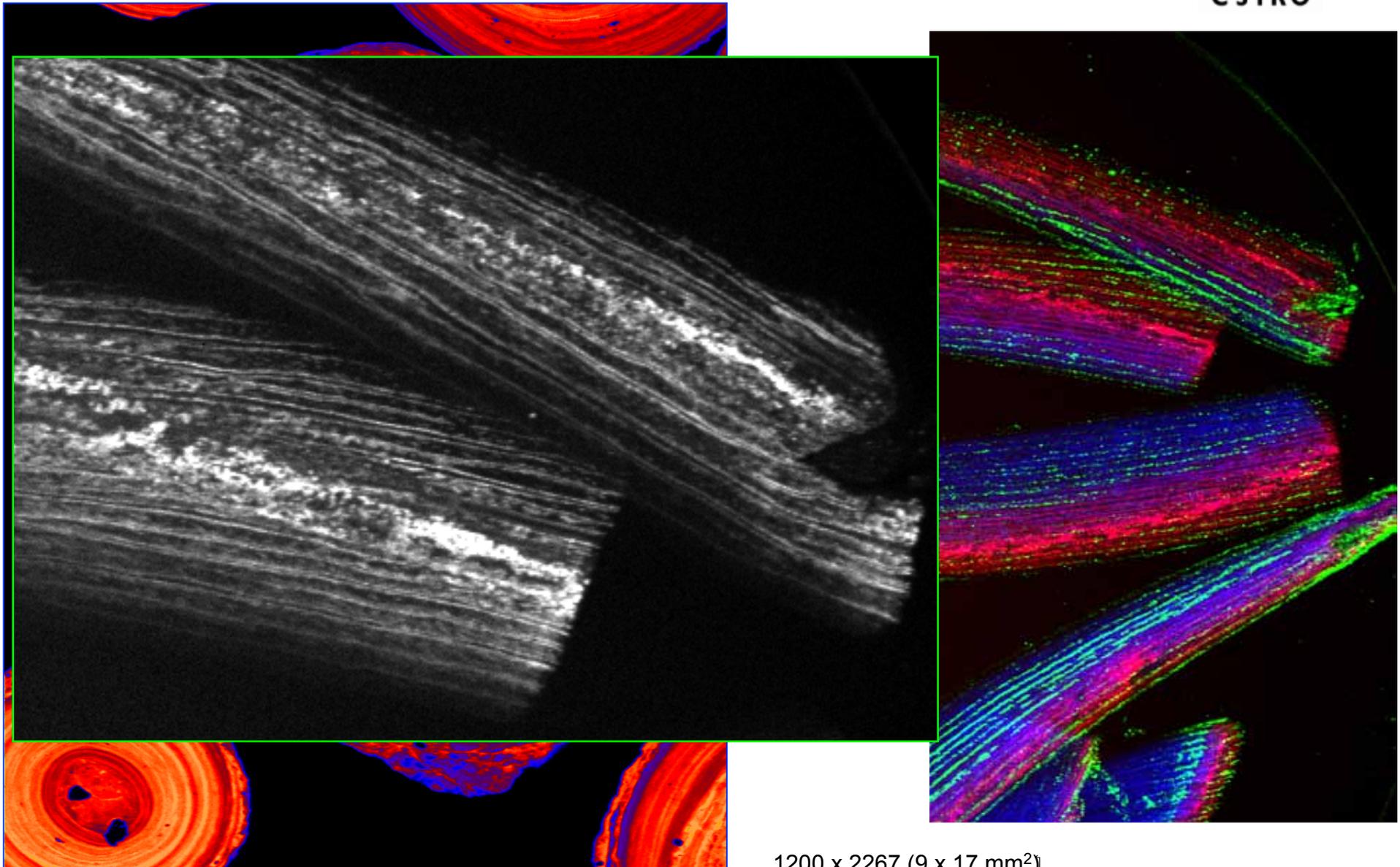
1200 x 2267 (9 x
17 mm²)
5.7 hours (7.5 ms
dwell)
7.5 x 7.5 μm² pixels



Rapid XRF Elemental Mapping (BNL/CSIRO collaboration)



Rapid XRF Elemental Mapping (BNL/CSIRO collaboration)



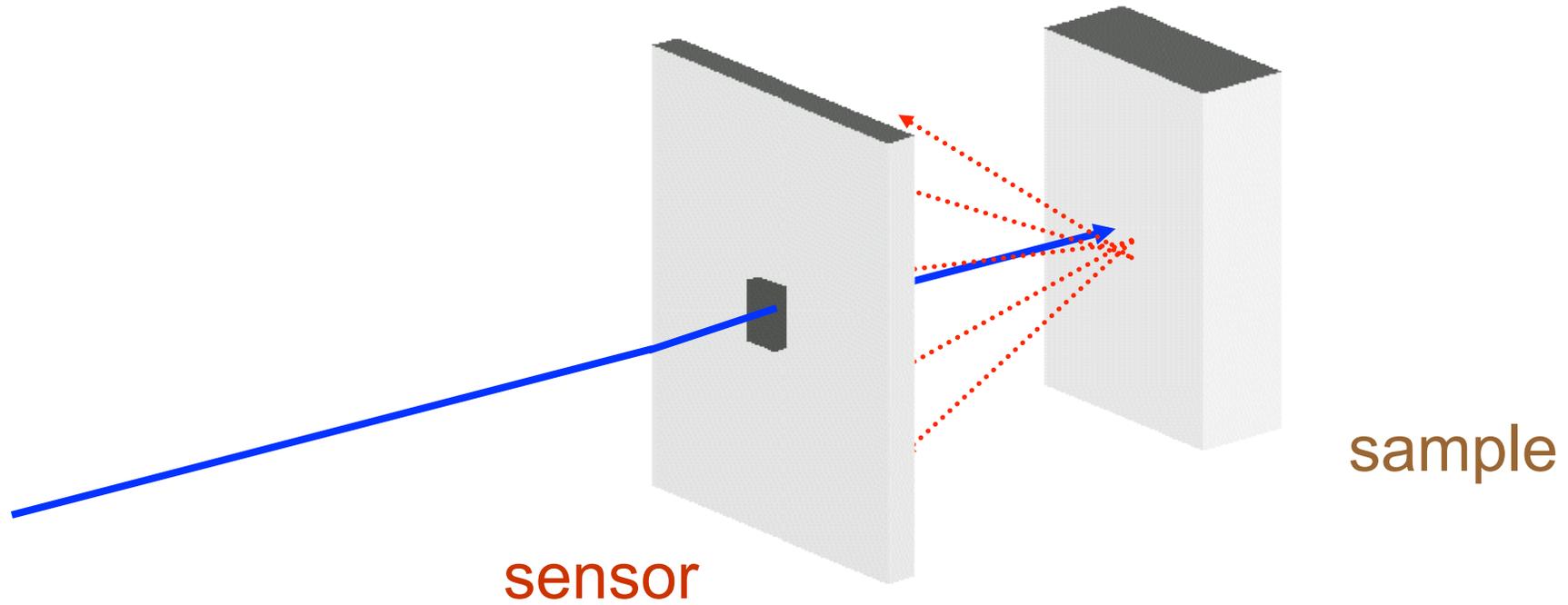
1200 x 2267 (9 x 17 mm²)

5.7 hours (7.5 ms dwell)

7.5 x 7.5 μm² pixels



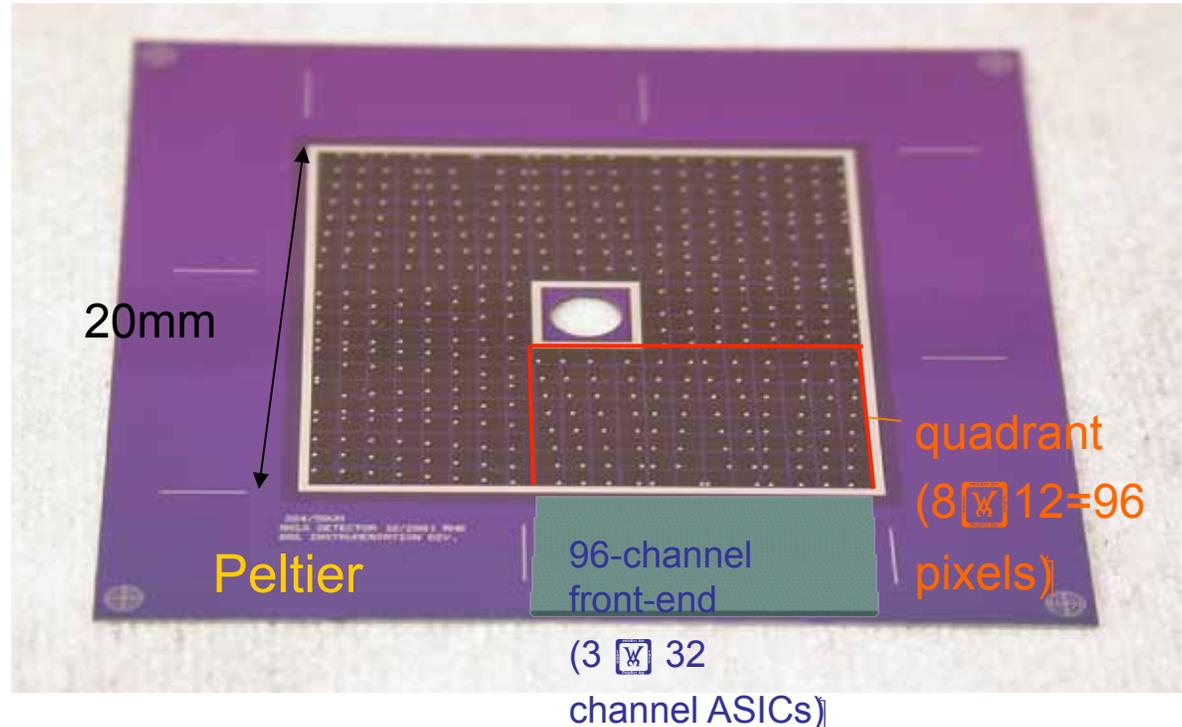
Backscattering geometry for fluorescence microprobe



- Backscattering geometry allows close approach to sample.
- Provides good solid-angle even for small detector area

High-rate multi-element detector for fluorescence measurements

- 384-element silicon pad array (1mm x 1mm) for absorption spectroscopy and/or x-ray microprobes.
- Central hole for incident pump beam to allow close approach to sample.
- >1 SR coverage
- Uses 12 Hermes +12 Scepters +CSIRO's Hymod FPGA system.

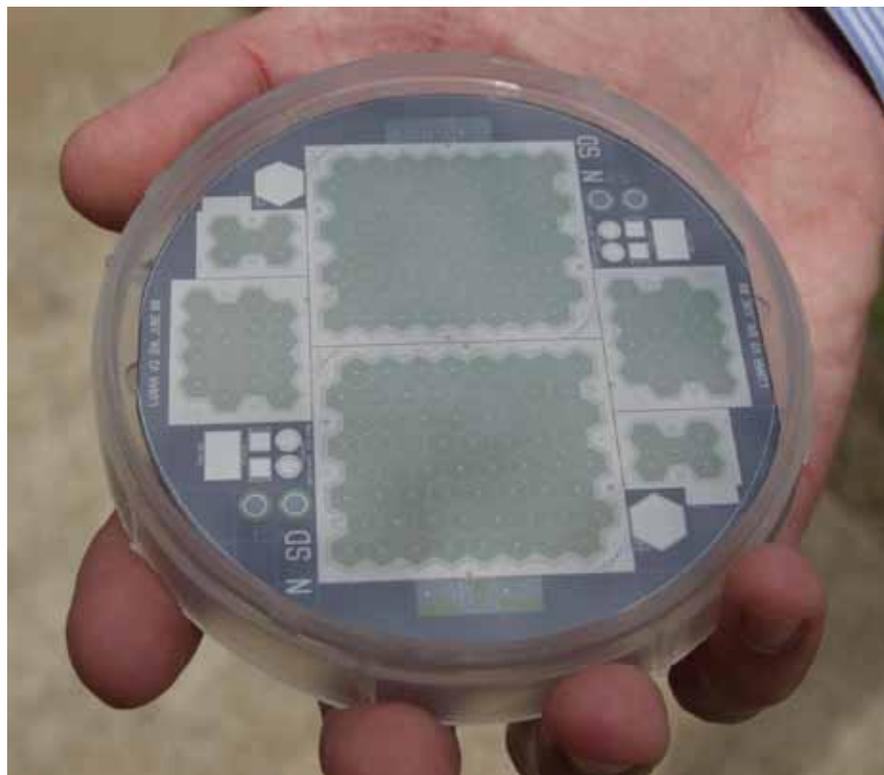


Moving forward with spectroscopy

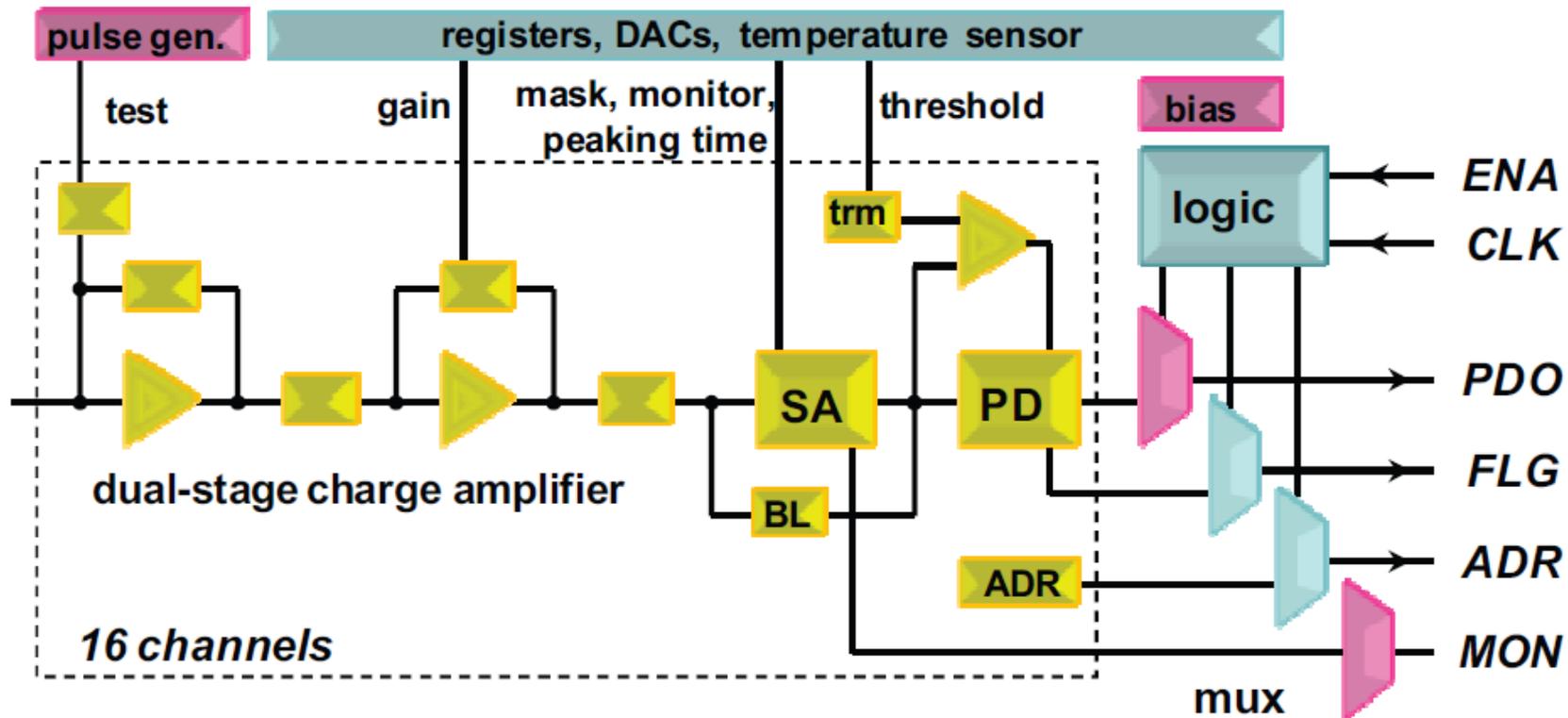
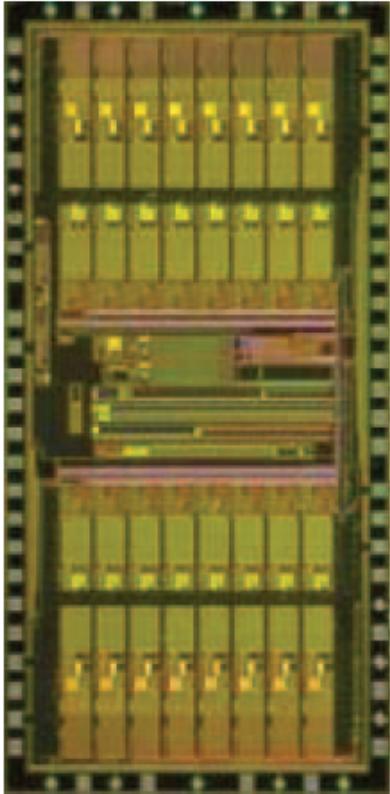
- NSF grant with Trevor Tyson (NJIT) to develop EXAFS and fluorescence holography detectors based on MAIA technology
- Will take MAIA and drift detector technology being developed for NASA and adapt it to EXAFS.

Rehak et al., NIMA, 2010, in press.

- NASA project will produce a 0.5m^2 array of drift detectors to fly in low-moon orbit, collecting x-ray fluorescence produced by solar wind. We have joined this project by helping with device testing, in exchange for access to detector arrays.
- Arrays of up to 64 SDDs have been successfully fabricated.
- Custom ASIC for SR applications under design



ASIC for SDD array readout



16-channel low-noise ASIC

Sparsified readout with peak-detector analog memory

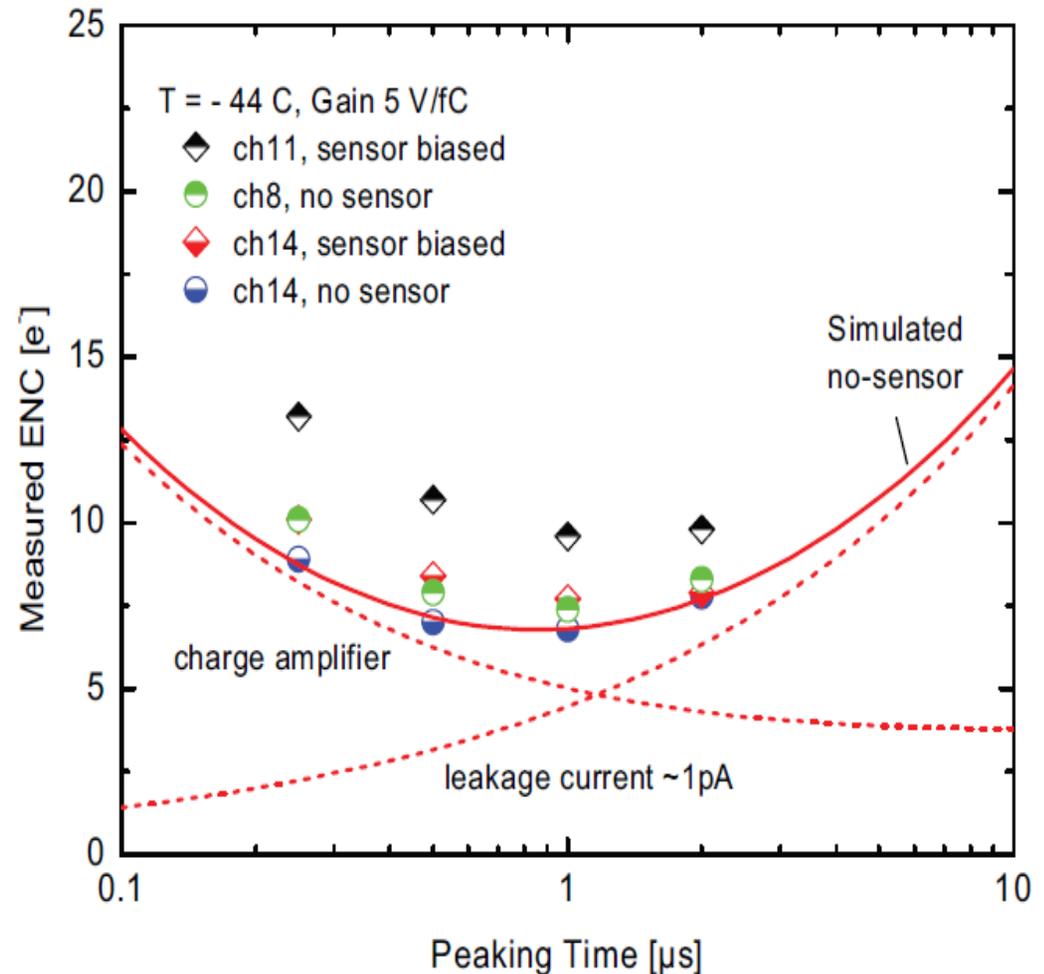
Low power, suitable for space applications

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 57, NO.

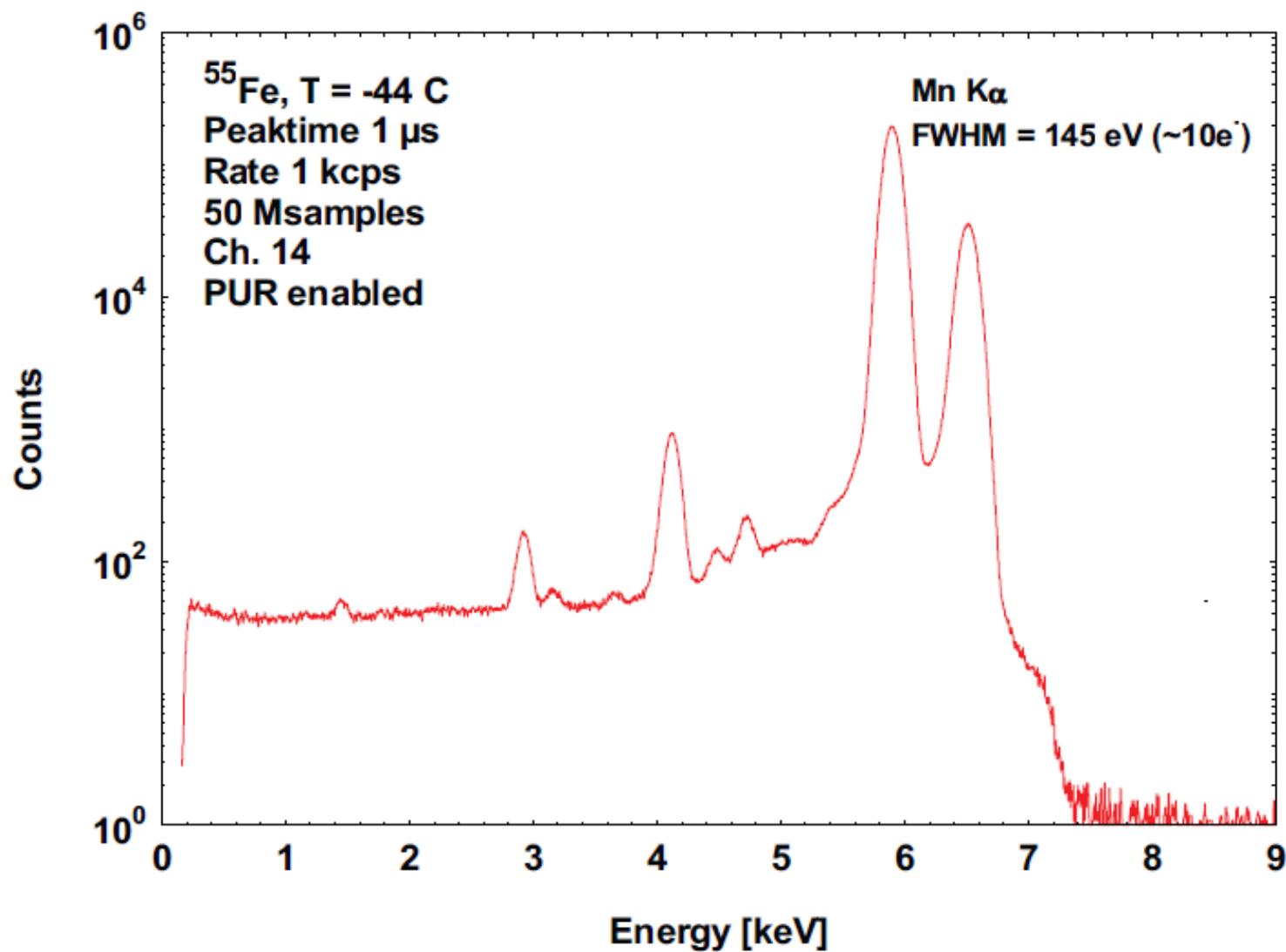
3, JUNE 2010, De Geronimo et al.

Noise performance

- Noise limited by stray capacitance and sensor leakage current.
- Best performance $\sim 8e$ rms @ 1 μ s shaping time.



^{55}Fe spectrum

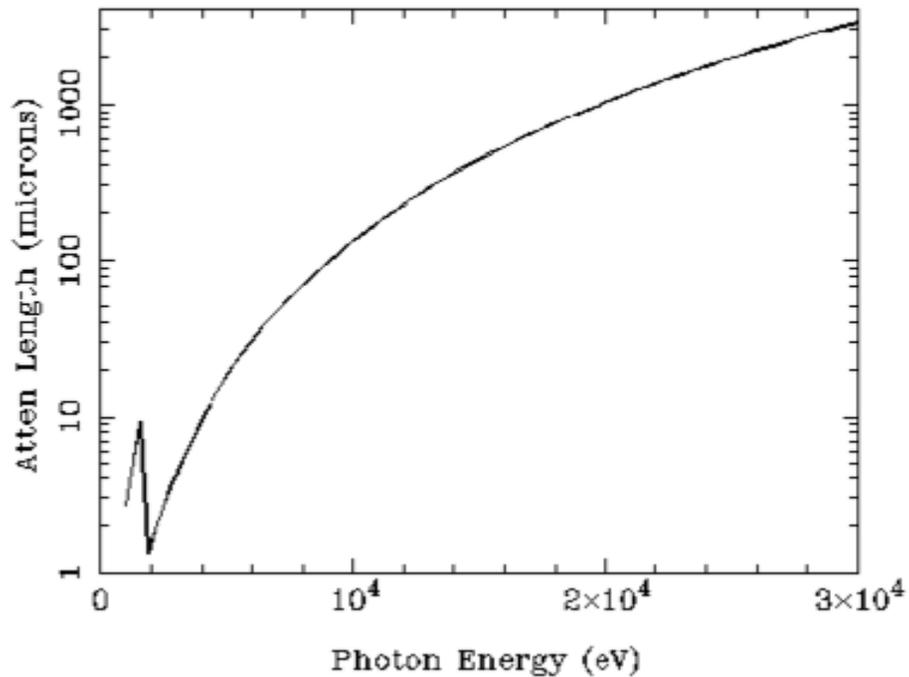


Outline

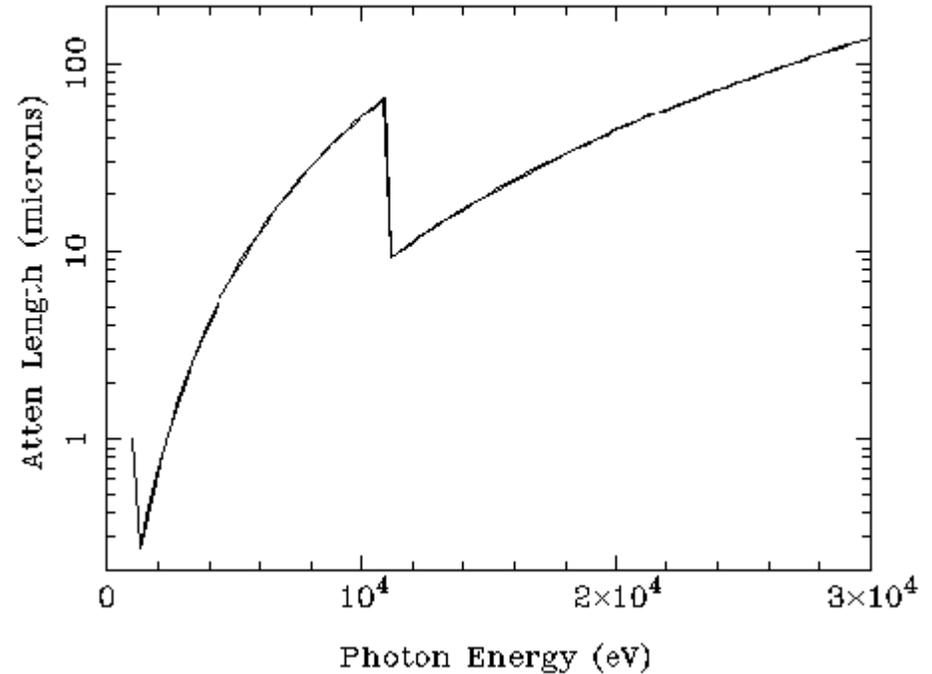
- BNL Projects
 - ☒ Spectroscopy
 - ☒ Germanium
 - ☒ Imaging
 - ☒ Future
- Summary

Absorption length for Si & Ge

Si Density=2.33, Angle=90.deg



Ge Density=5.323, Angle=90.deg



- Materials science needs $E > 20\text{keV}$ to penetrate dense materials (alloys, ceramics etc.)
- Biology needs higher E to reduce radiation damage

Germanium

- Aim to develop planar process for germanium
 - ☒ High quality insulation and passivation coating
 - ☒ Ion implantation recipes for n-type and p-type species.
- Industry is re-examining germanium for its high carrier mobility.
 - ☒ Significant R&D on how to integrate germanium technology into mainstream production.
 - ☒ We will adapt this work to suit our purpose.
 - Need low-temperature process steps to prevent problems with hydrogen evolution from detector-grade germanium
 - n-type implant is problematic
 - So-called Hi-K dielectrics look promising for use as an insulating layer for germanium

Band offset of HfO₂ on Ge

Improper band offset would give rise to higher leakage current

HfO₂ on SiC for example would not work as a good oxide due to low band offsets [1]

Furthermore, need to understand what surface passivation (either N or S) does to the band offsets.

Dependence of the charges at the interface and the oxide charge to the band offsets

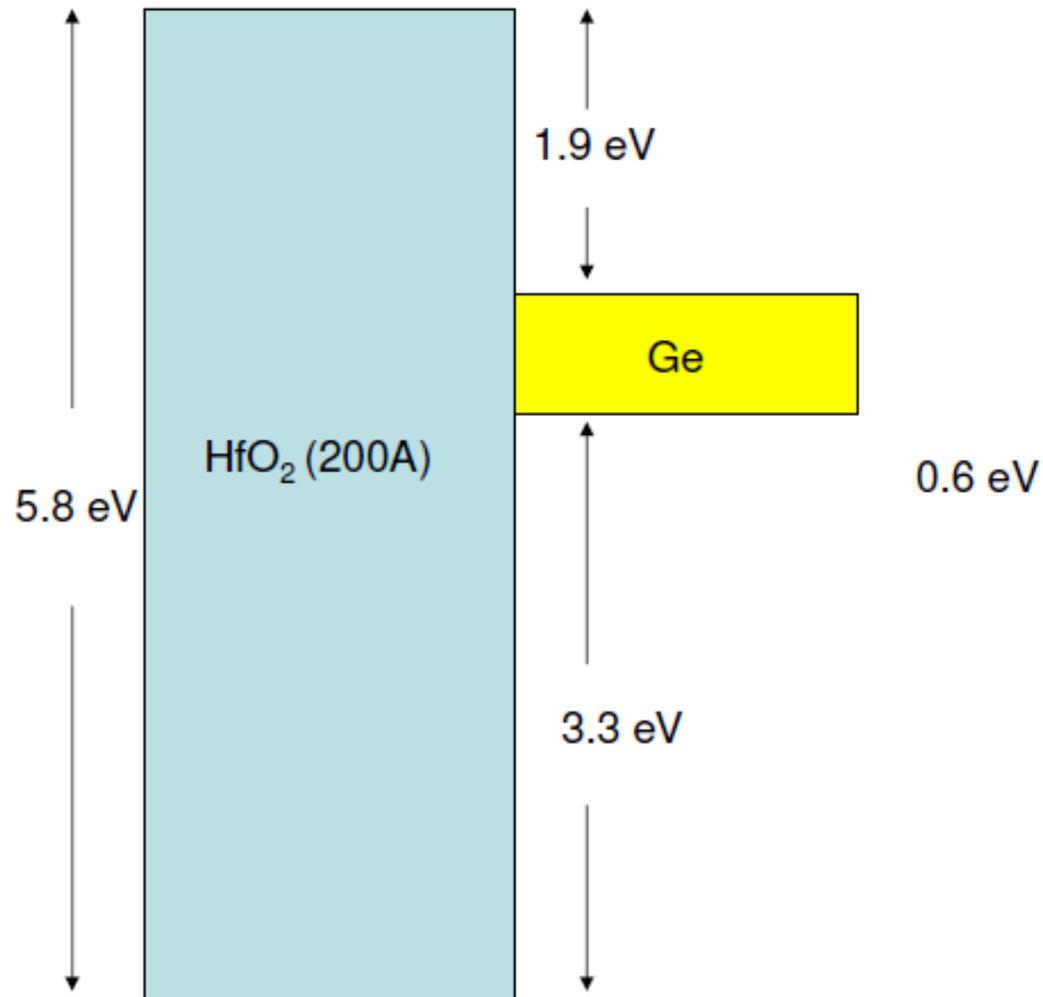
1. R. Suri, C. J. Kirkpatrick, D. J. Lichtenwalner and V. Misra, *Appl. Phys. Lett.*, **96**, 042903 (2010).

Comparison of Hf core level after alignment of Ge 3d core

**No change in band offset although
The oxide charge and the interface
charge are found to be higher in N
passivated Ge !**

(A. Rumaiz et al, submitted).

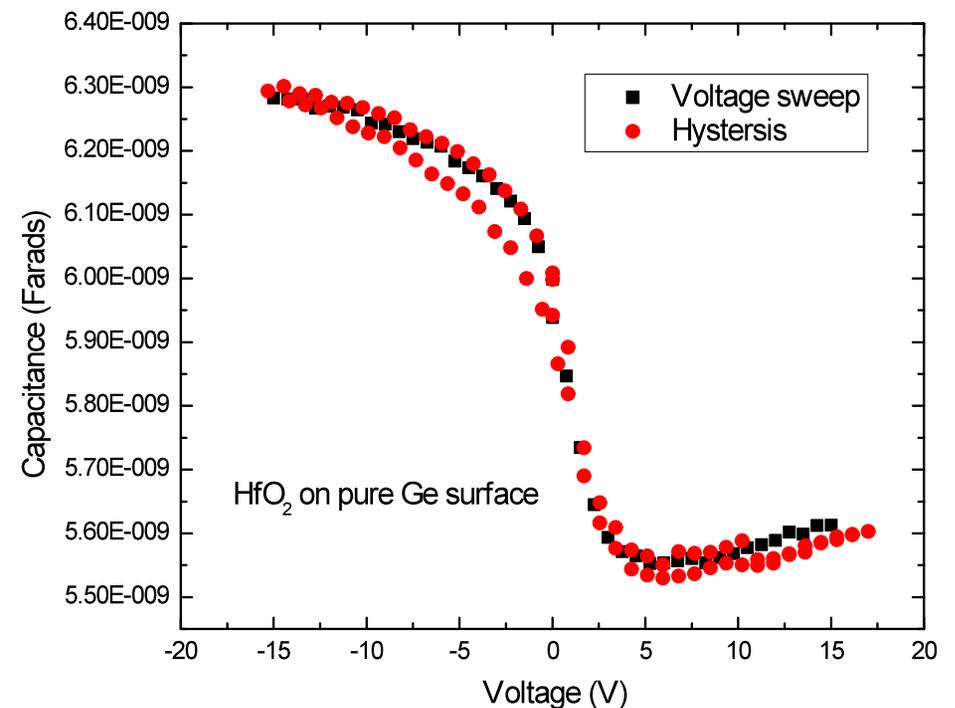
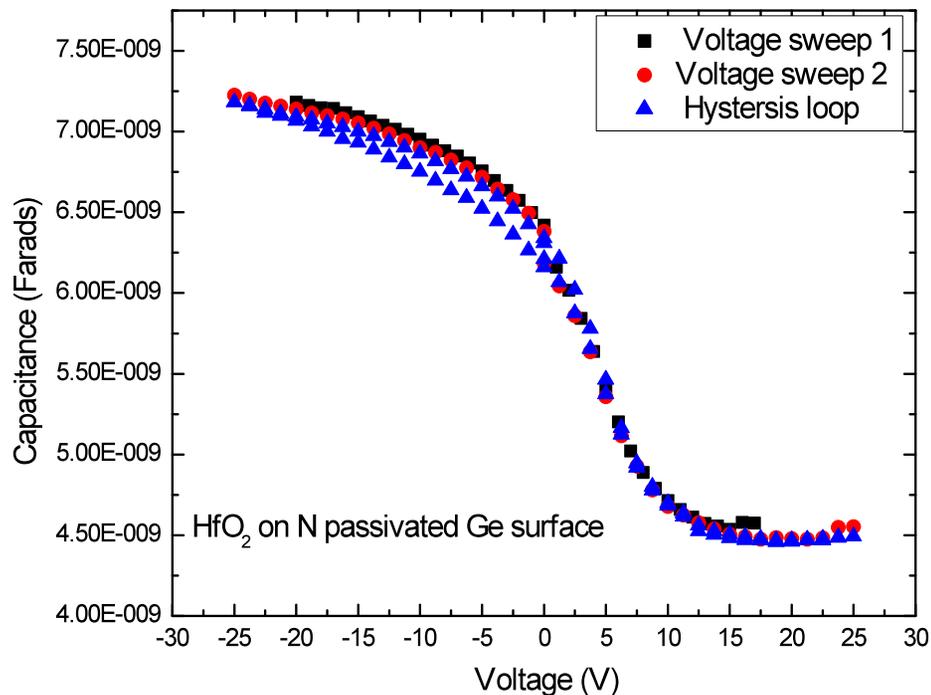
Calculated band offsets



Most interestingly the offset seems Independent of the oxide/interface Charge !!!

System Studied

C-V curves for ALD grown HfO_2 on clean and N passivated Ge.



Oxide charge of about 3V but lower hysteresis

Oxide charge of about 1V

Conclusions and path forward

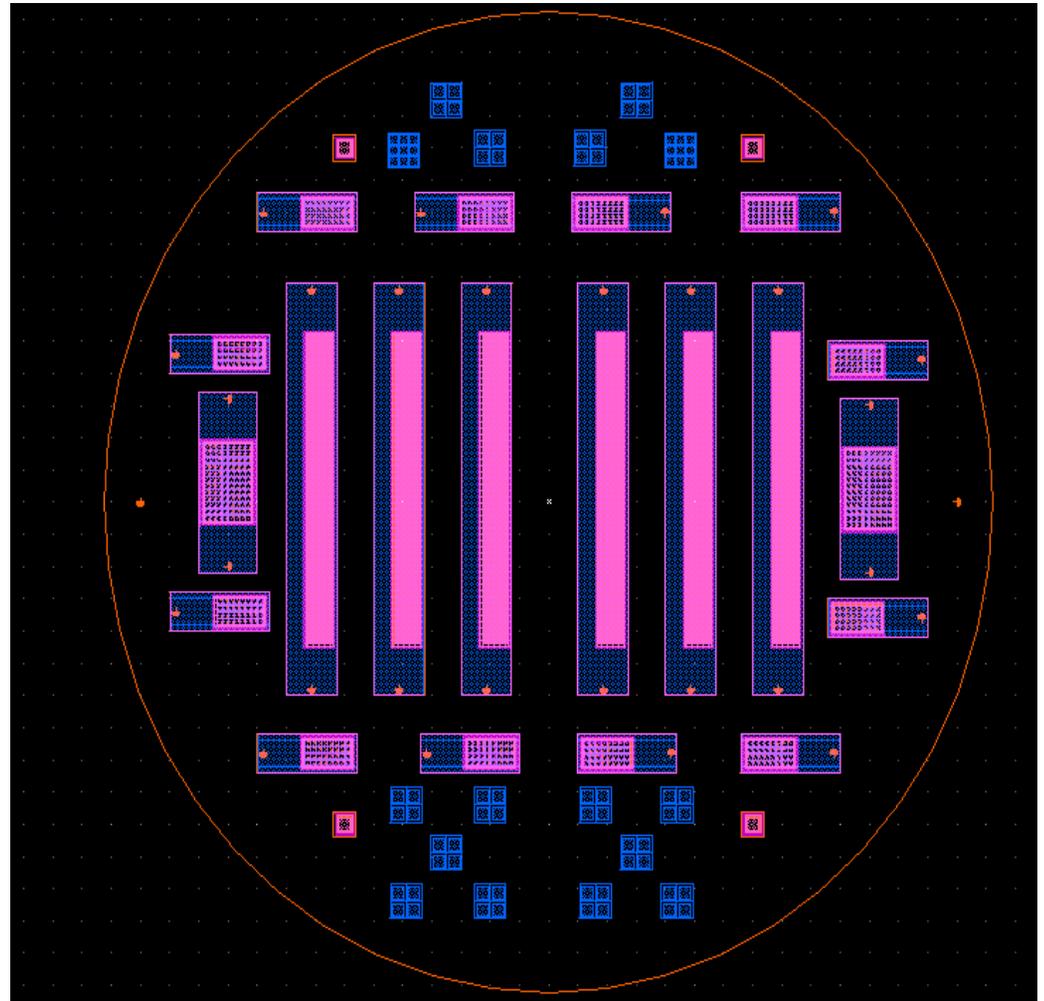
- The measured band offsets are sufficiently large to consider HfO_2/Ge as a stable oxide for both electrons and holes based device applications.
- Band offsets insensitive to the interface charges

Path forward

- Implant B on both sides for pixel isolation (blanket implant through SiO_2 as capping layer)
- Remove SiO_2 and deposit high K (HfO_2) by atomic layer deposition at Cornell nano Facility
- Lithograph windows for P implant. HfO_2 passivation layer would be protected by photoresist to prevent doping of the high K oxide.
- Activate implant by rapid thermal anneal.
- Metallization followed by final litho...

First mask set for pixellated planar monolithic Ge detectors (we hope!)

Simple diode arrays
in the form of pads
and strips, similar
to ones we have
made in silicon.



Outline

- BNL projects
 - ☒ Spectroscopy
 - ☒ Germanium
 - ☒ Imaging
 - ☒ Other
- Summary

Specifications for LCLS detectors

- Source: 100fs pulses at 120Hz -> no photon counting, so need integrating detector.
- Two applications with very different specifications:

☒ X-ray Pump-Probe

- ~100% efficient @ 8keV
- < 1 photon readout noise
- 10^4 photons full-well
- ms readout time (< 8ms)
- Extremely challenging spec: $>10^4$ S/N, single-shot, fast readout.

☒ X-ray Photon Correlation Spectroscopy

- 100 photons full-well
- $\ll 1$ photon readout noise, needs different technology
- ms readout time.

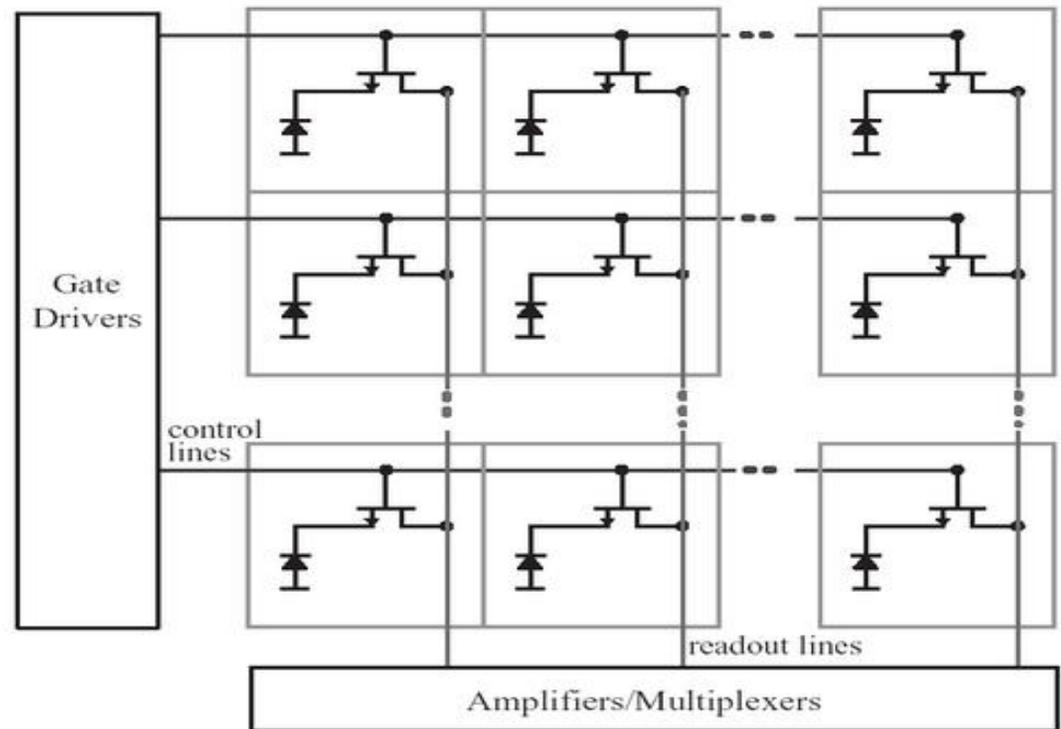
Monolithic construction

Monolithic devices built on fully-depleted high-resistivity silicon provide simplest structure

- No bump-bonding
- Fully depleted wafer -> good efficiency
- Simplest structure is monolithic active-matrix type
 - Switching mechanism integrated with sensor
 - Small pixels in principle possible (no on-pixel amps)
 - row-by-row parallel readout by off-sensor amplifiers
 - N readout channels instead of $N \times N$, modular readout from edge of detector by a few (~ 16) small ASICs
- Need to develop technology to form transistors directly on high-resistivity silicon substrate.

LCLS detector: Active matrix readout

- Charge stored in diode capacitance (switches off)
- Readout amplifier/ADC on each column
- Switches turned on sequentially row-by-row
- Charge read out and digitized
- 1us per row => 1ms for 1000 rows.
 - ☒ 8-channel 20MHz/channel ADC
 - ☒ 8 chips, each ADC multiplexed among 16 columns
 - ☒ 2Gb/s data rate



Pixel structure

- Low-resistivity layer is formed by deep implant.
- JFET switches are fabricated in this layer
- Charge is produced by photo-ionization
- Electrons collect under pixel (switch is OFF)
- Charge is read out by turning transistor ON, connecting stored charge to a buss-bar, and read out by a charge-sensitive amplifier.

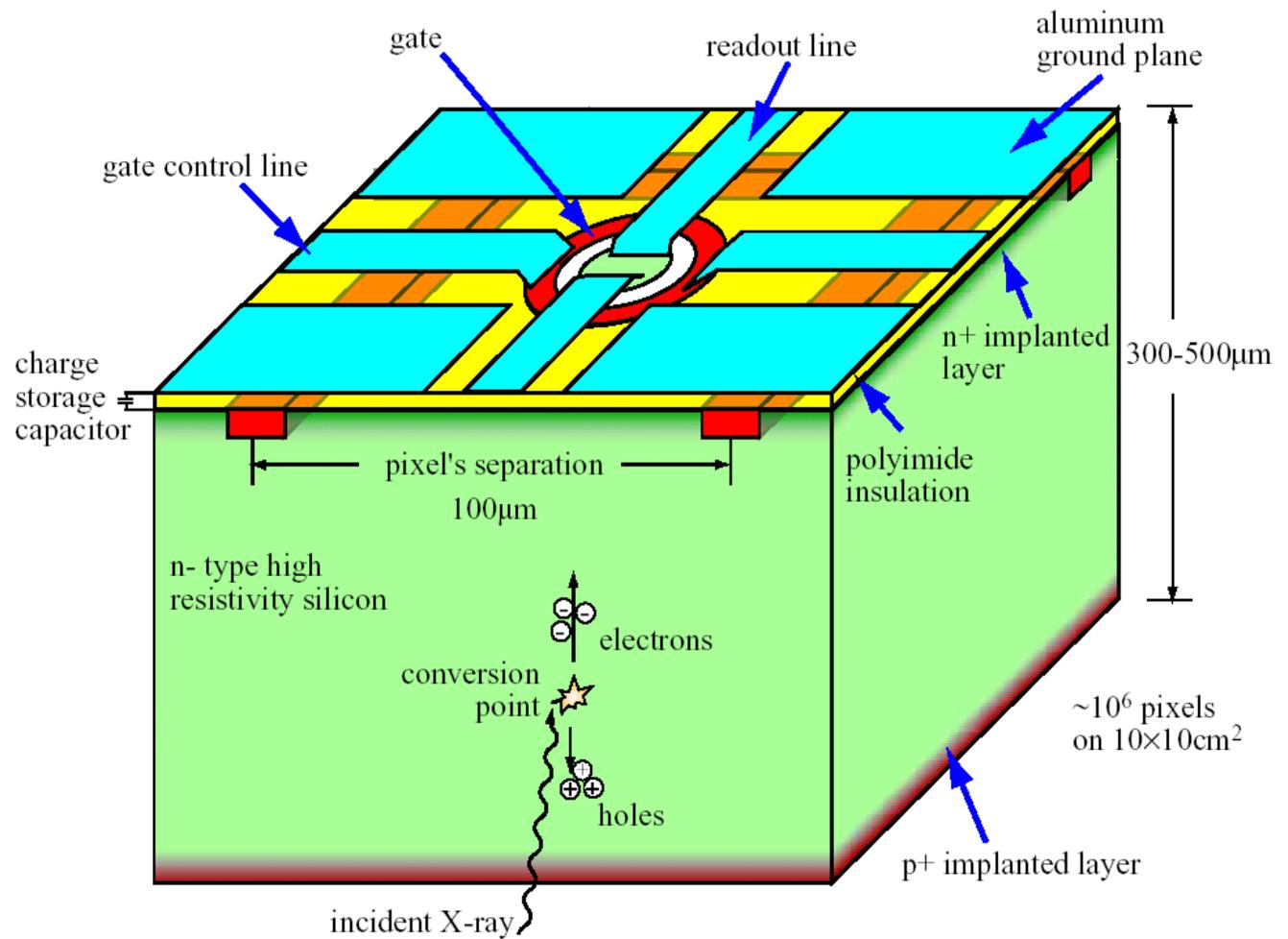
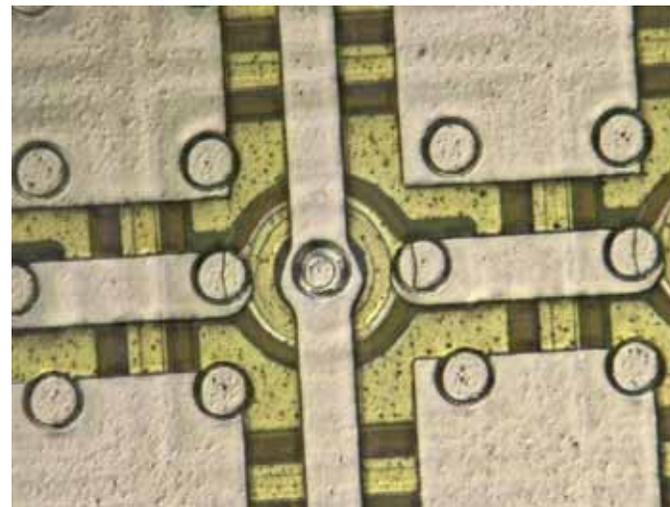
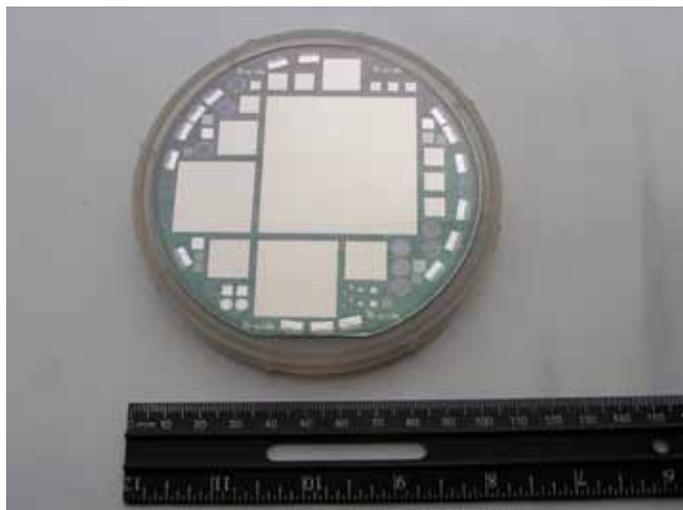


Figure 6. One pixel from an Active Matrix Pixel detector array. The device is fabricated by forming a low-resistivity silicon layer suitable for JFET switching devices on top of high-resistivity silicon optimized for detector fabrication. The JFET transistors formed in this layer are used to row-sequentially switch the collected charge into column output amplifiers.

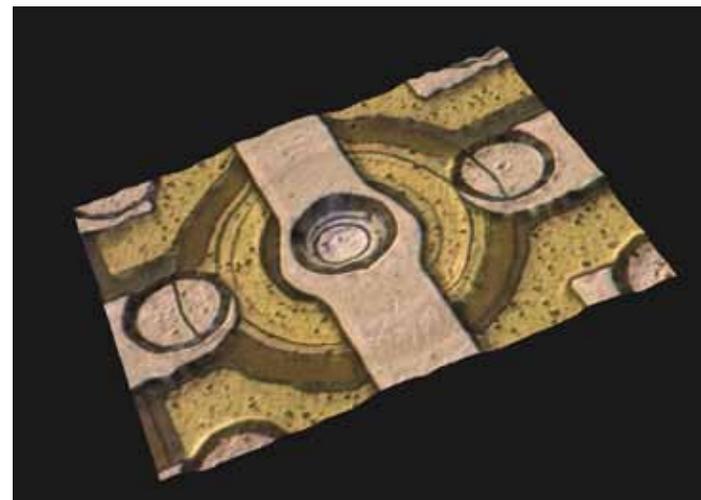
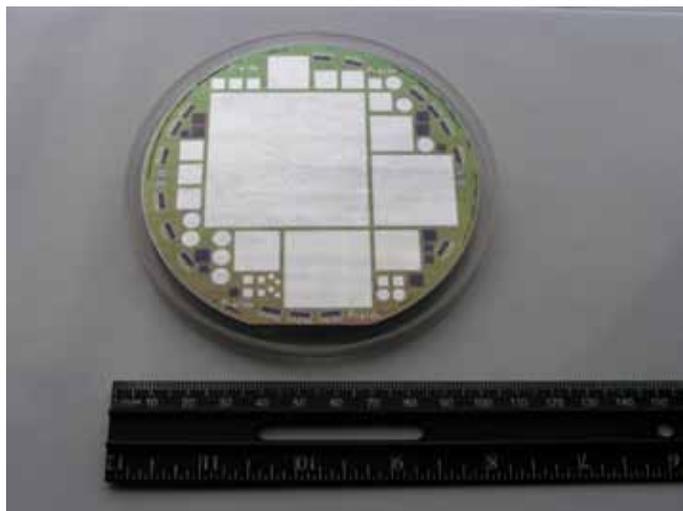
Final wafers

Device side



Details of a pixel

Window side



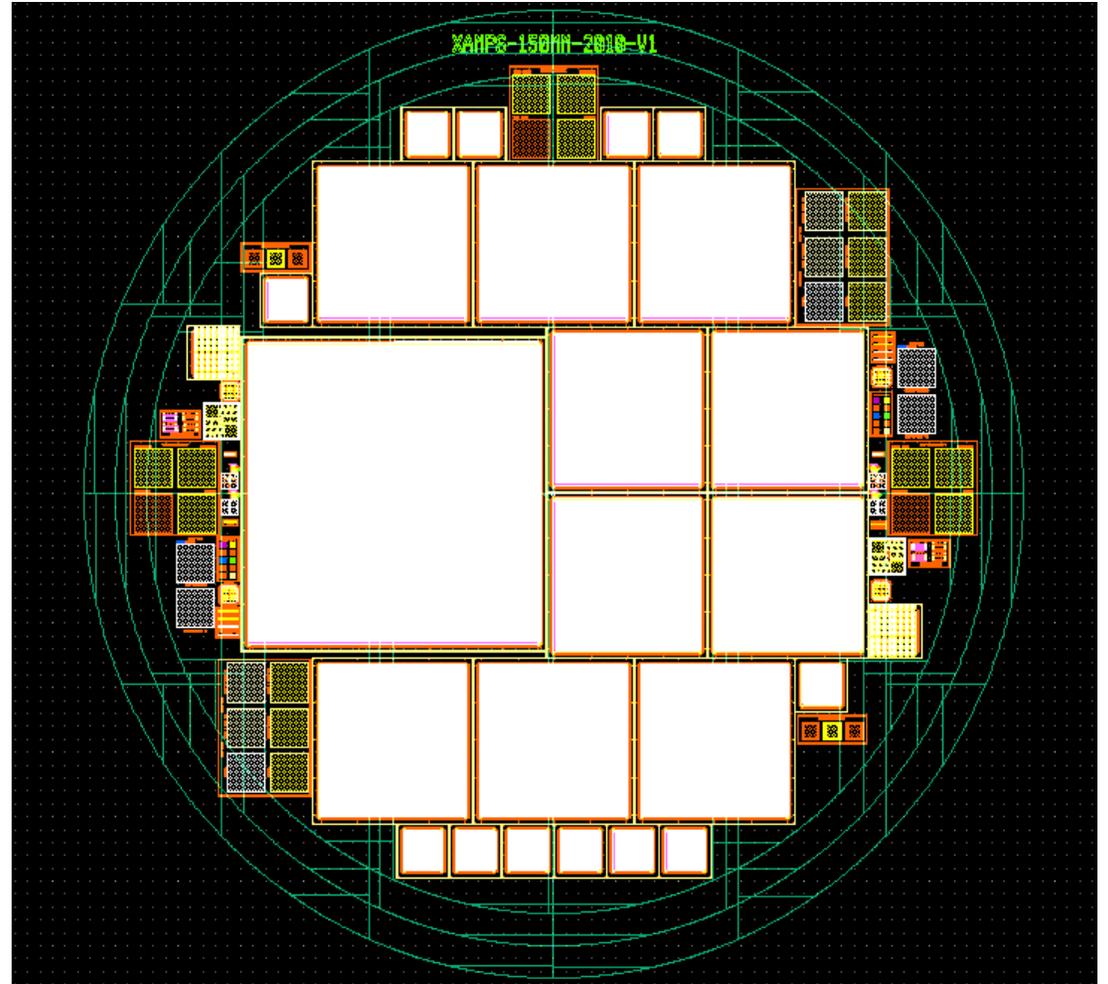
6" wafer mask for new production

Focus on 256x256
device

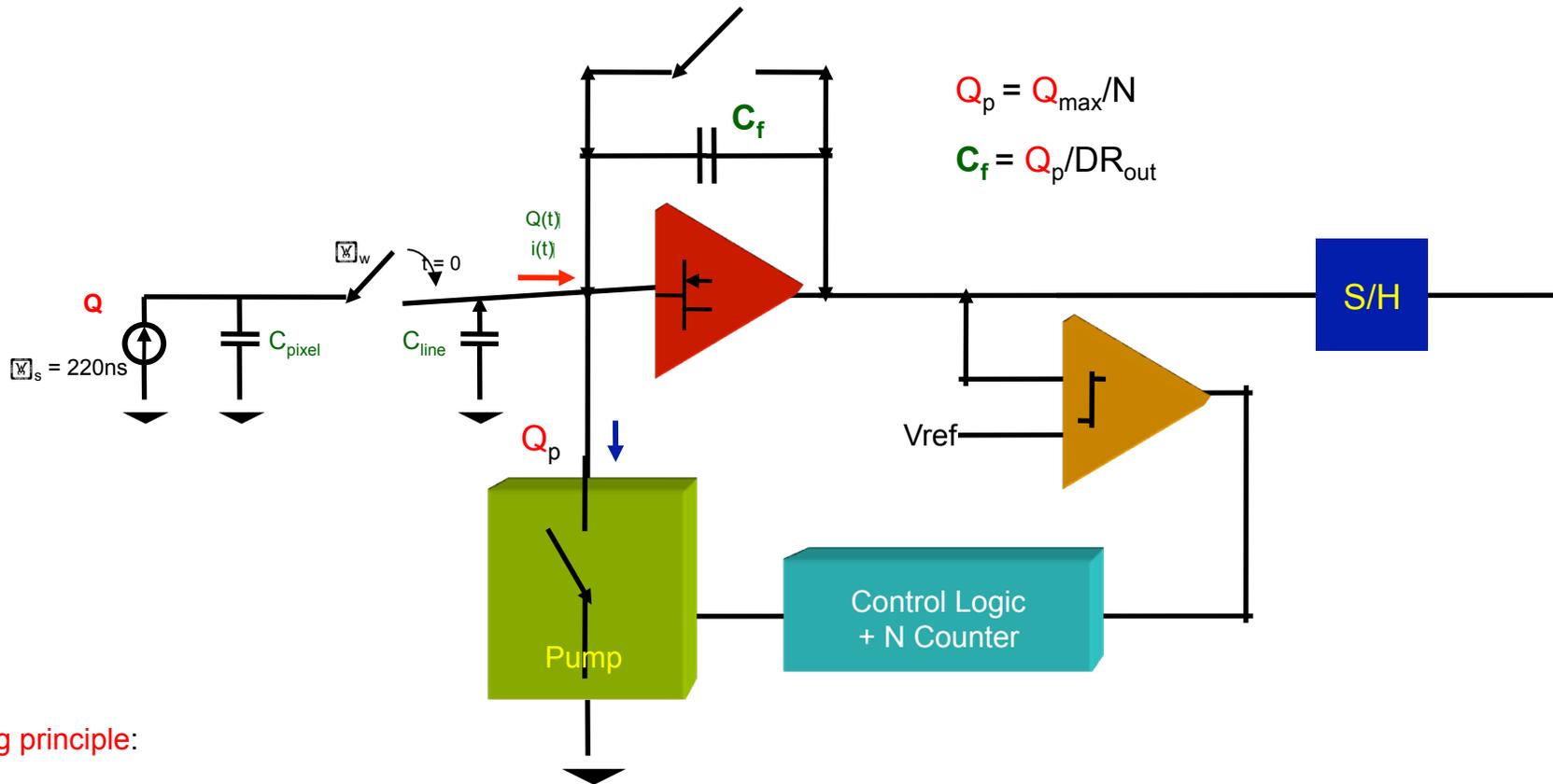
Fabrication to be
done by Ketek,
Munich.

Array of 16 devices
will form full
detector

(1024x1024)



Readout ASIC: Charge Pump or 0 Balance Method

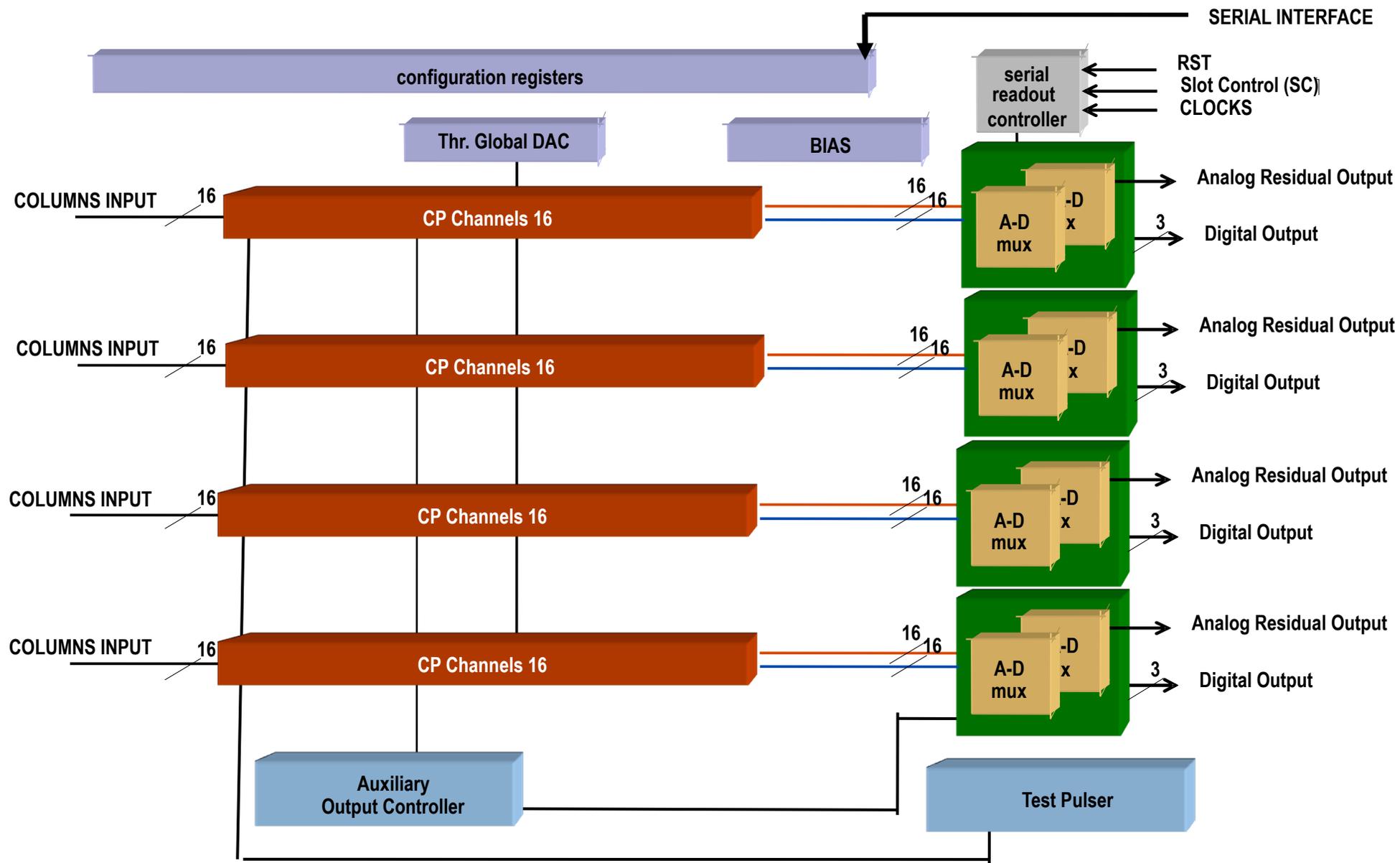


Working principle:

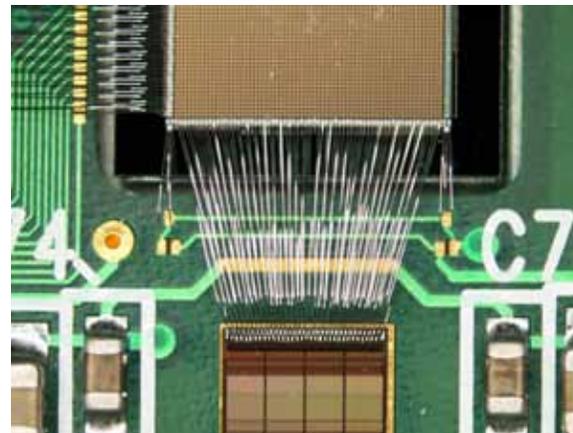
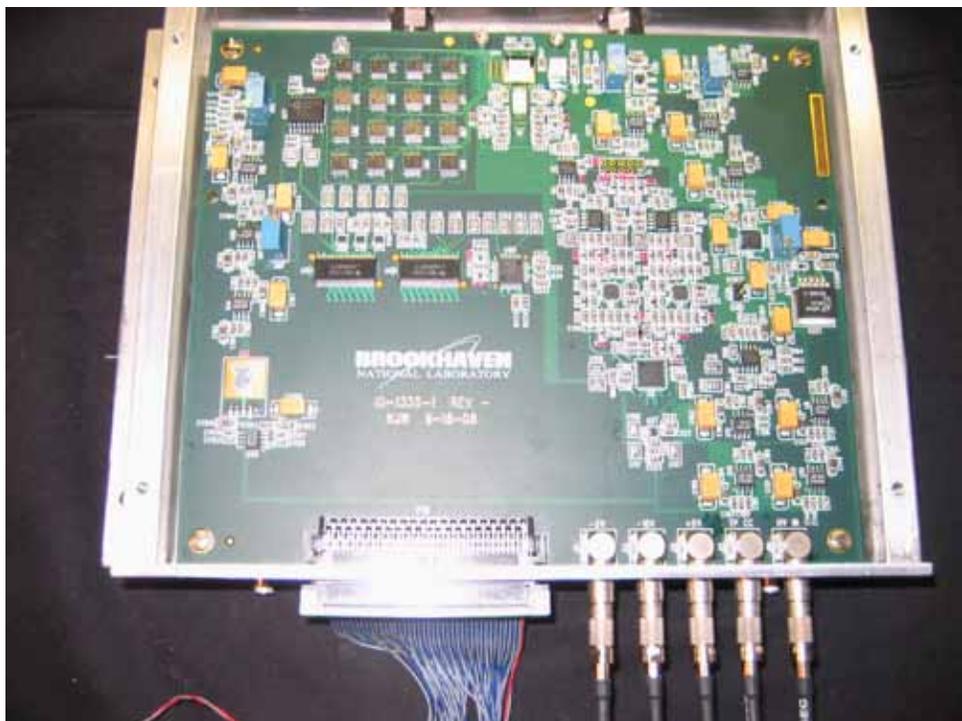
To meet the required resolution over the entire dynamic range a 0 balance method is applied: the dynamic range is divided in N ranges each one corresponding to a charge $Q_p = Q_{\max}/N$. When a charge larger than Q_p is presented to the input a charge pump is activated to remove fixed amount of charge equal to Q_p until a residual smaller than Q_p remains stored in the feedback capacitor C_f . The number of charge quanta Q_p removed by the pump are counted and the corresponding digital value is presented at the output representing the most significant bits of the final A/D conversion (for $N=16$ we have 4 bits).

The residual charge in the feedback capacitor is then sampled according to a CDS scheme, presented at the output and converted with a 14bit ADC (total of $14+4=17$ bits).

ASIC Architecture



Test board - DAQ



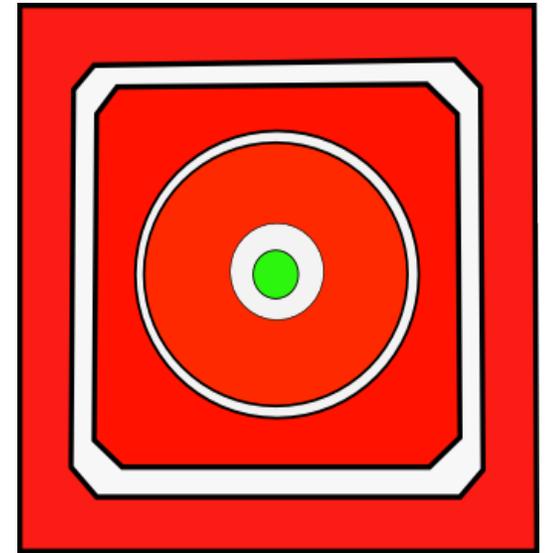
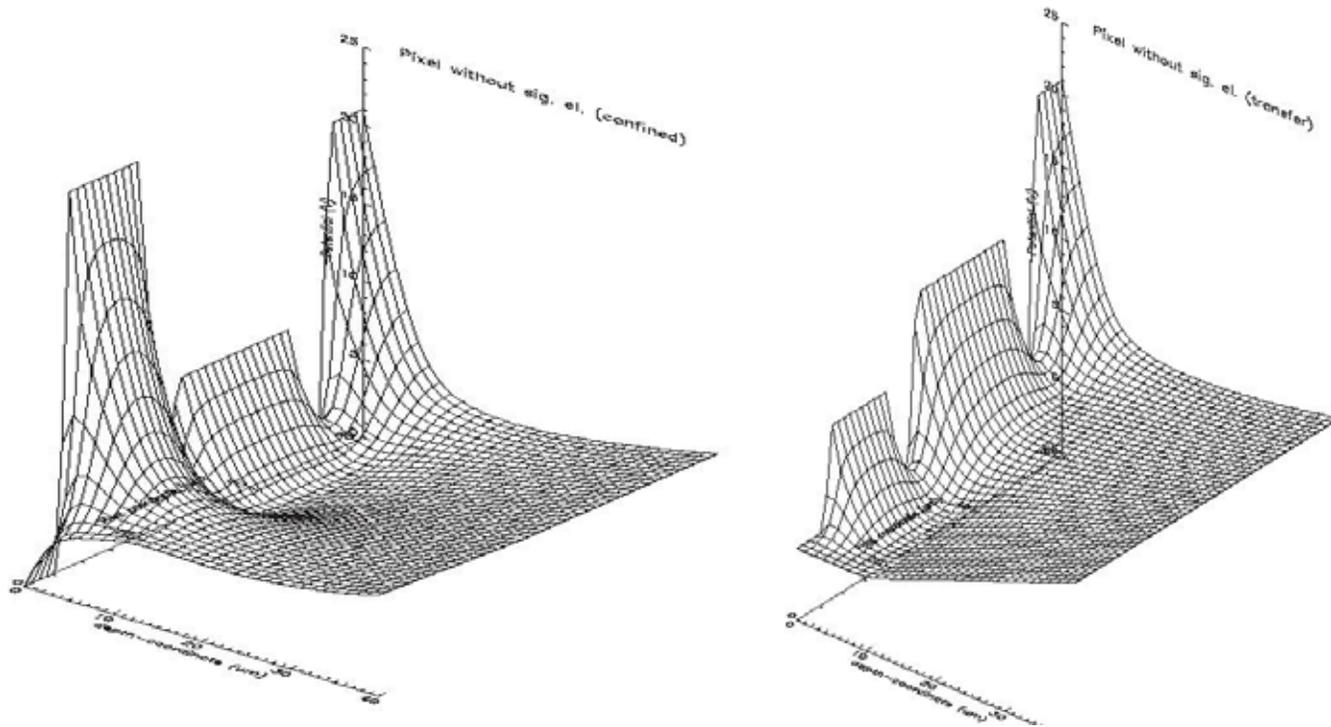
DAQ

- FPGA prototyping board with
- 4 channels, 14 bits,
 - 20 Msamples/s ADCs
 - 64 x 64 pixel sensor
 - 1 FEXAMPS ASIC

Charge Pump Detector

- XCS experiment requires lowest possible noise, but moderate capacity.
- New design keeps simplicity of XAMPS but avoids switches and hence kTC noise.
- Uses drift-detector concepts pioneered by Rehak and Gatti.

Charge pump pixel



Charge is accumulated in potential well formed by biasing of the three implanted regions.

It can be released into an amplifier by changing the biases on the inner two structures.

See poster by G. Carini et al.

Outline

- BNL Projects
 - ☒ Spectroscopy
 - ☒ Germanium
 - ☒ Imaging
 - ☒ Future
- Summary

Future developments

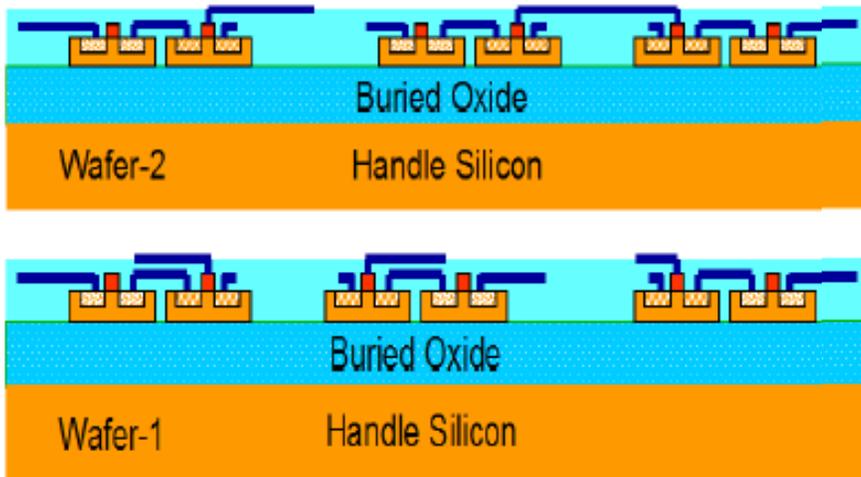
- Need to provide more functionality on-pixel
 - low-noise spectroscopy ($<20e^-$)
 - deep fast time framing / readout
 - time-correlation spectroscopy
- 3D integration?

Process flow for 3D CMOS Chip

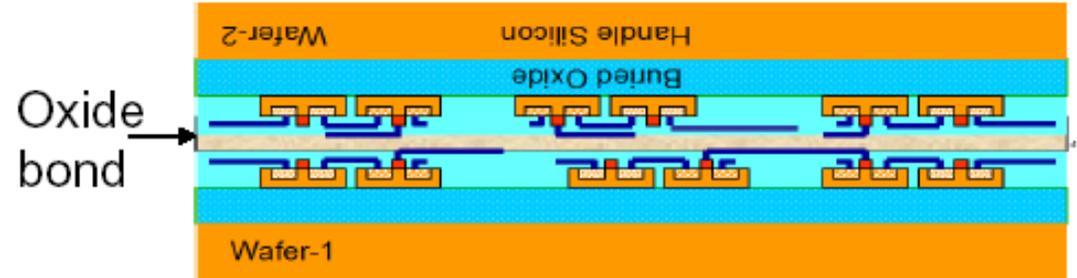
(Courtesy Ray Yarema, Fermilab)

- 3 tier chip (tier 1 may be CMOS)
 - 0.18 um (all layers)
 - SOI simplifies via formation
- Single vendor processing

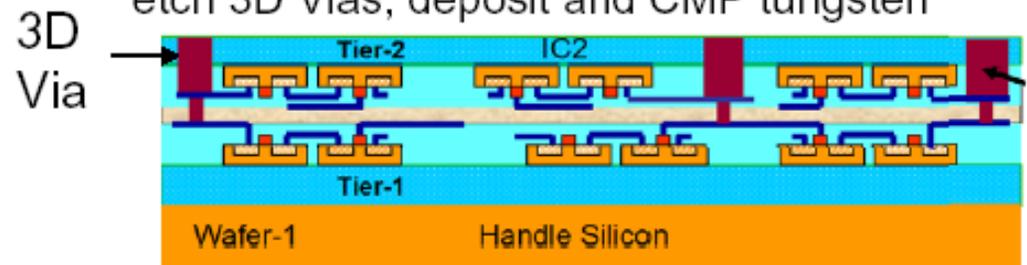
1) Fabricate individual tiers



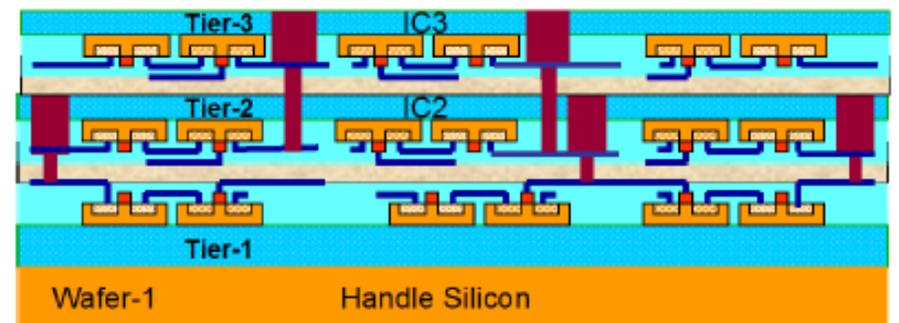
2) Invert, align, and bond wafer 2 to wafer 1



3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



Issues

- CMOS foundries can't handle high-resistivity ($\sim 10\text{k ohm-cm}$) wafers
 - ☒ Thermal budget issues
 - ☒ Wrong size wafers
- This forces a 2-vendor solution
 - ☒ Sensors made on 6" HR wafers (at BNL)
 - ☒ 3D chips bonded to sensor wafers by low-temperature process
- We have chosen to work with Tezzaron / Chartered for 3D CMOS and Ziptronix for bonding sensors.
- Collaboration between BNL, Fermilab and AGH UST, Krakow, Poland

VIPIC

Fermilab ASIC Group, USA

Grzegorz Deptuch, Marcel Trimpl,

Raymond Yarema

AGH UST, POLAND

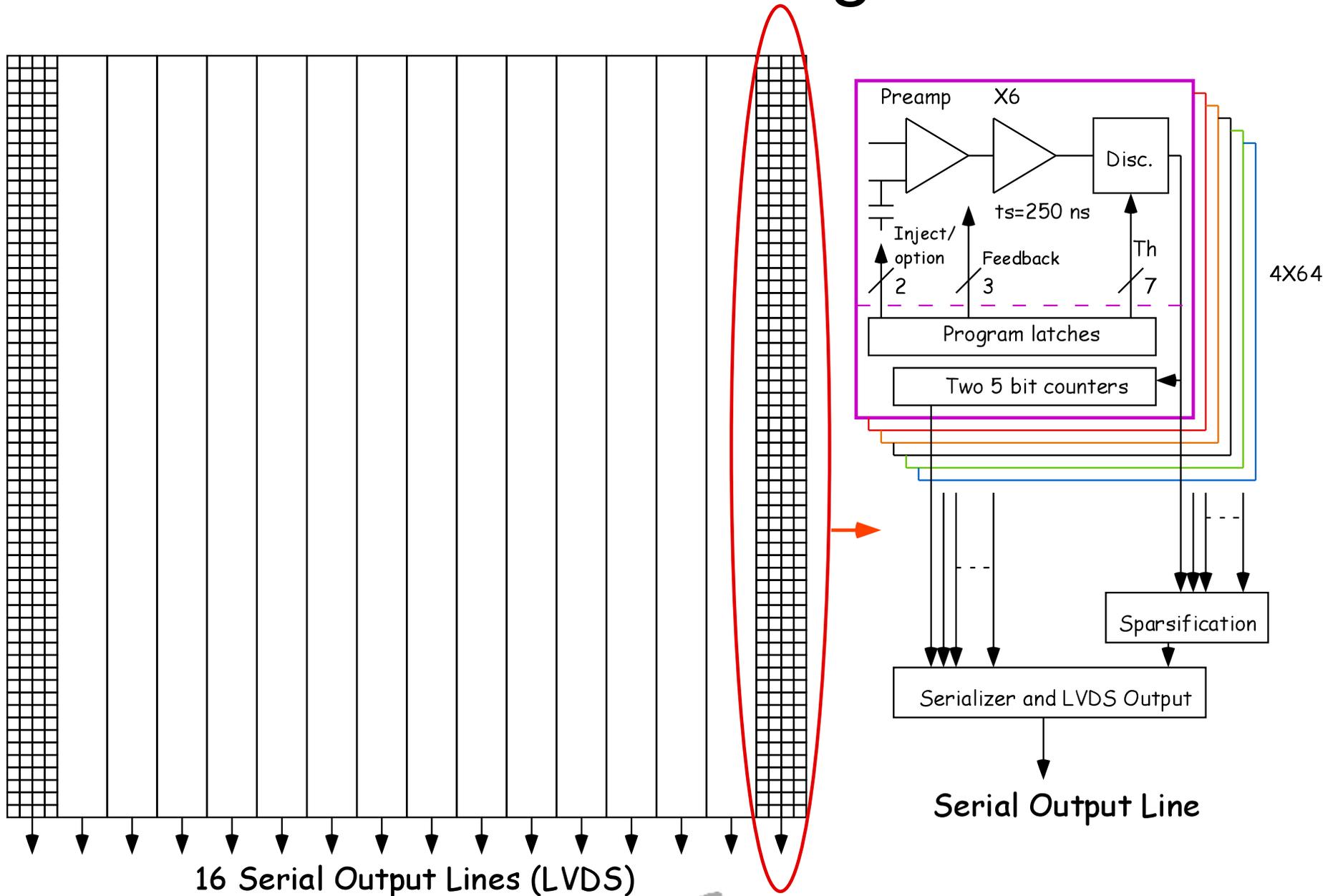
Pawel Grybos, Robert Szczygiel,

PhD students: Maciej Kachel, Piotr Kmon

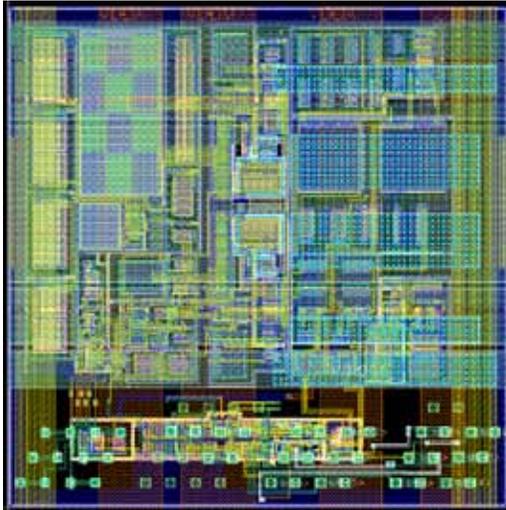
VIPIC (Vertically Integrated Photon Imaging Chip)

- Specifications
 - 64 x 64 array of 80 micron pixels
 - Dead timeless operation
 - Sparsified data readout
 - Binary readout (no energy information)
 - High speed frame readout time (10 usec min for occupancy ~ 100 photons/cm²/usec)
 - Optimized for photon energy of 8KeV
 - Triggerless operation
- Features (5.5 x 6.3 mm die size)
 - Two 5 bits counters/pixel for dead timeless recording of multiple hits per time slice (imaging mode)
 - Address generated by circuit without hard coding
 - Constant pixel address readout time (5 ns) regardless of hit pixel location by means of binary tree principle.
 - Parallel serial output lines
 - 16 serial high speed LVDS output lines
 - Each serial line takes care of 256 pixels
 - 2 tier readout chip with separate analog and digital sections
 - Adaptable to 4 side buttable X-ray detector arrays

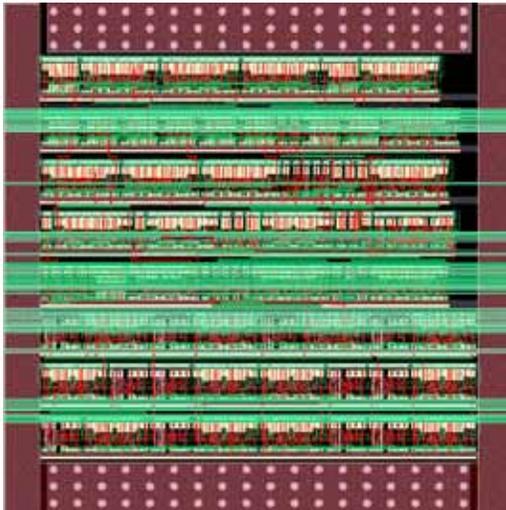
VIPIC Block Diagram



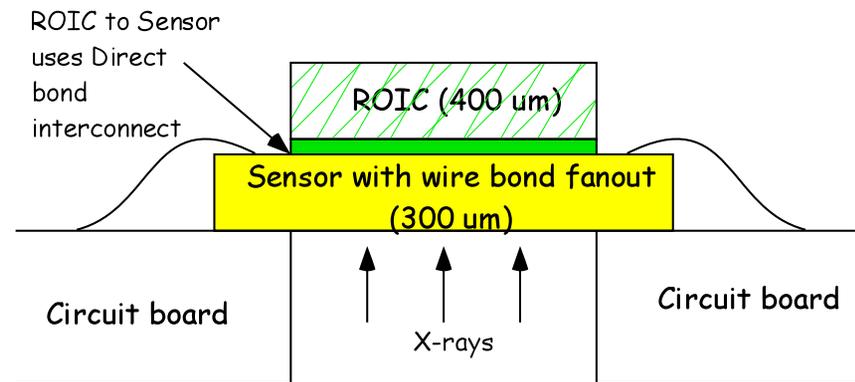
Pixel Tier Layouts and Sensor Mounting Options



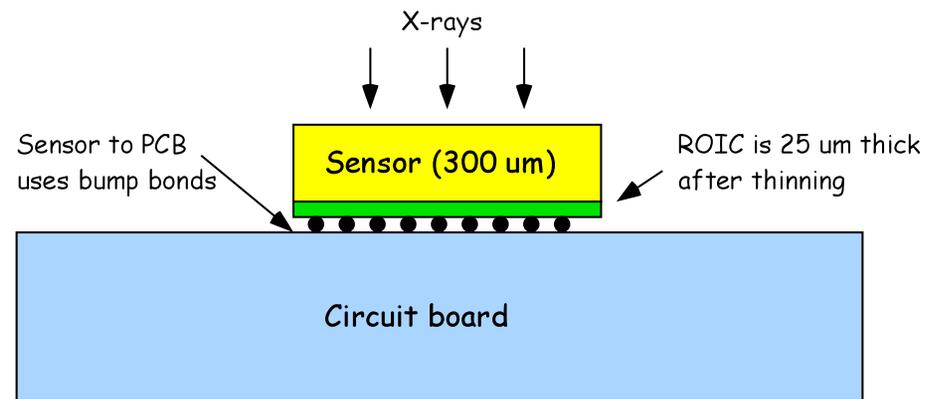
Analog Pixel Tier



Digital Pixel Tier



Option 1 - Less Aggressive Mounting



Option 2 - More Aggressive Mounting
for four side buttable sensor arrays

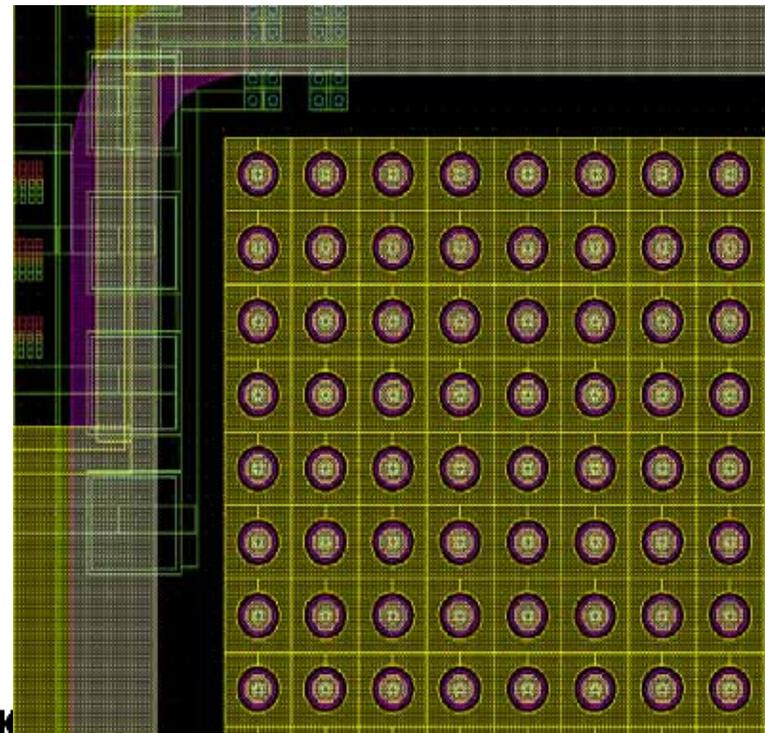
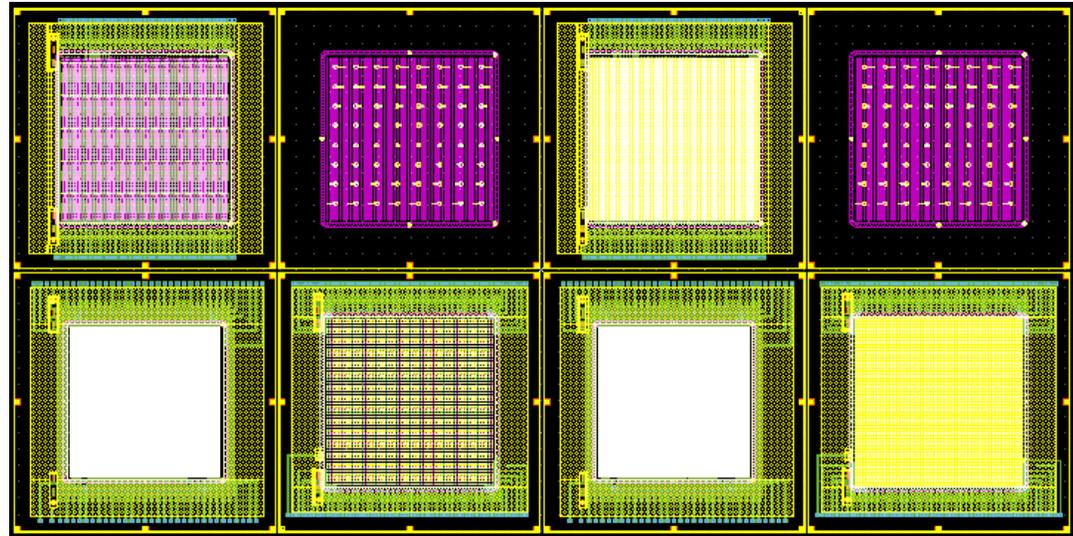
Sensor design

VIPIC sensor is part
of a multi-project
run

Eight sensor
designs on same
wafer

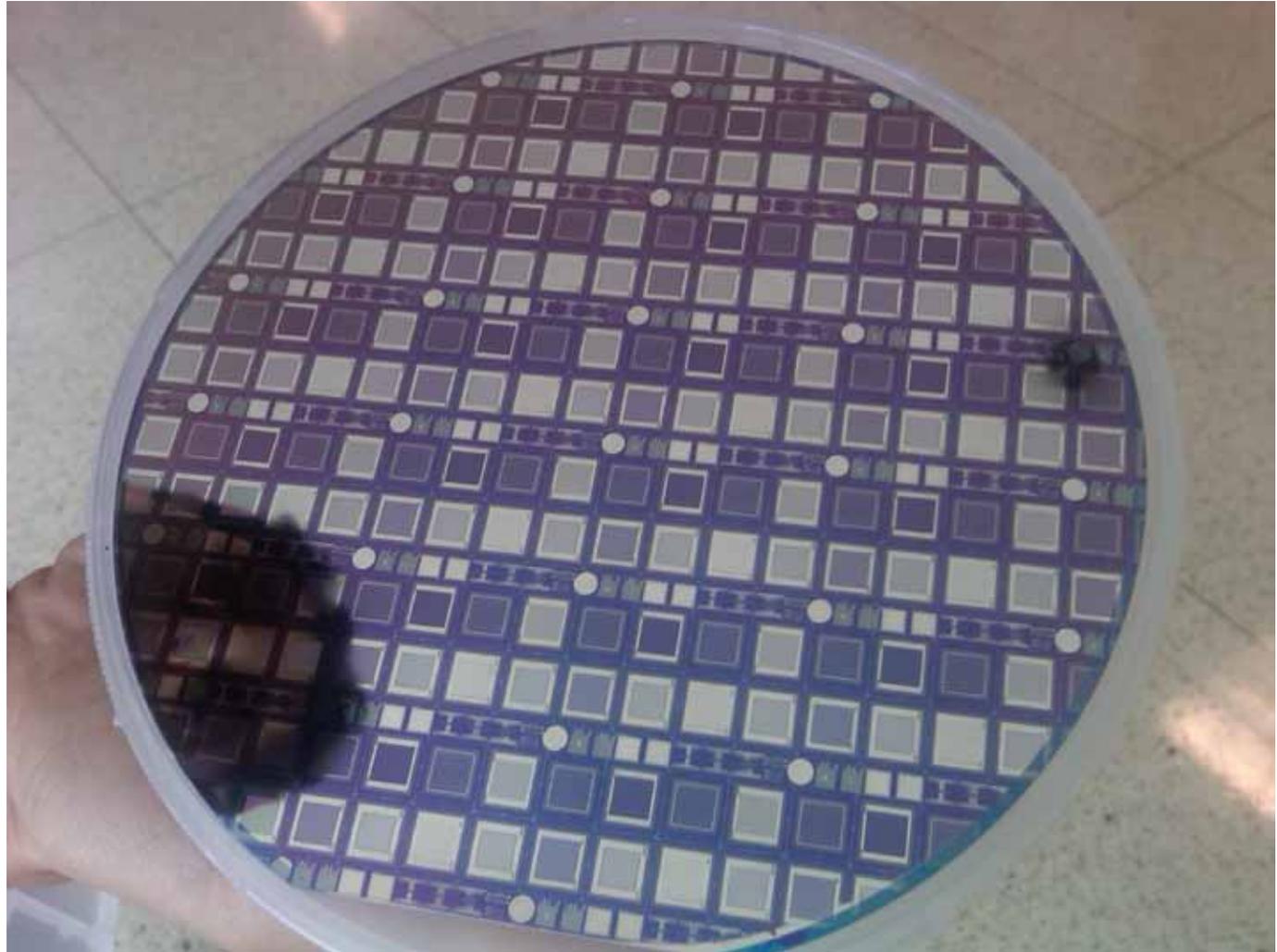
Two of them are
VIPIC, one with
shield and one

without.



Sensor wafer

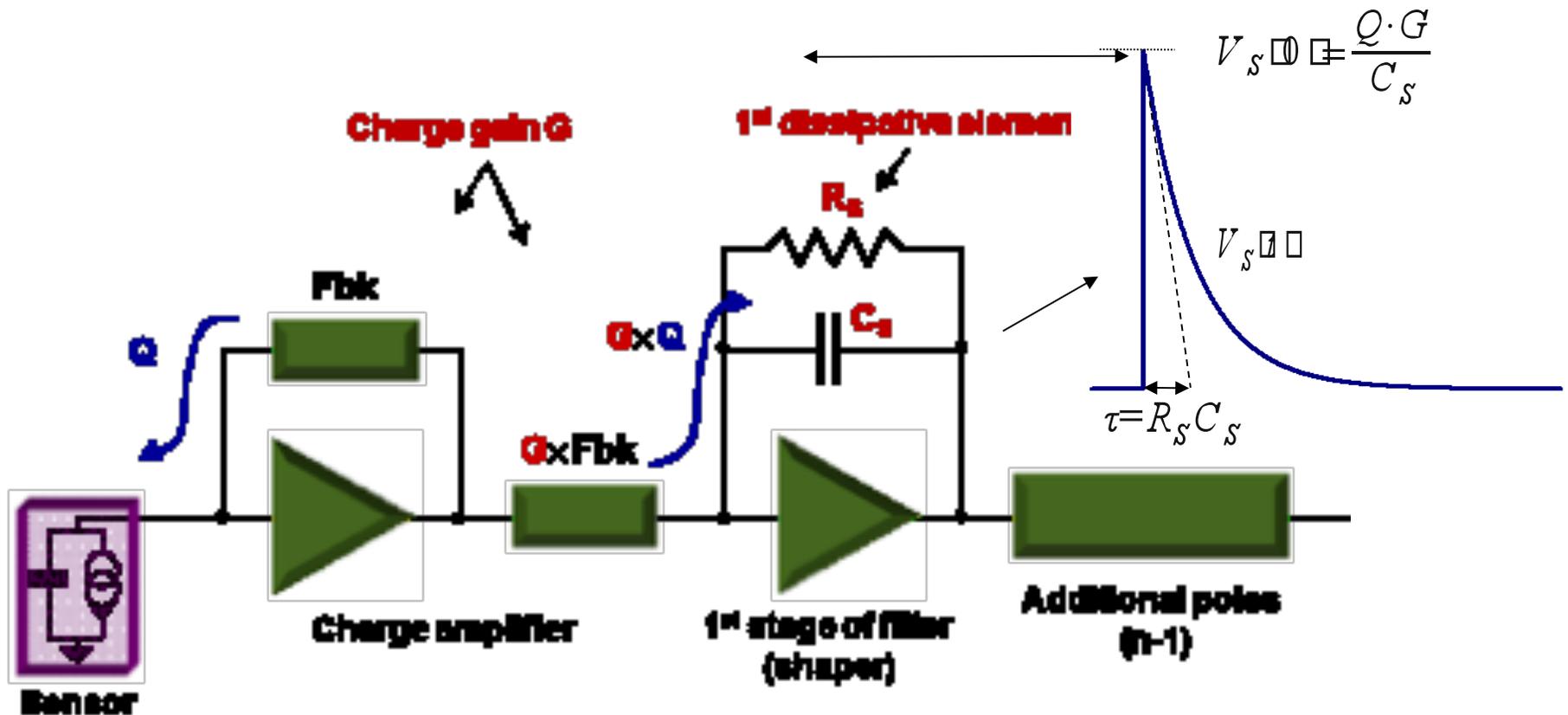
- 6" wafer
- Reticle contains 8 small sensor arrays.
- 3D ASICs will be bonded to each array.



Energy-resolving imaging detector

- Most often-requested detector is an area detector with energy resolution in every pixel.
- We have begun to evaluate how 3D-integration might provide a solution.
- Start with optimizing analog section and sensor
- Prototype test will use only one CMOS layer with TSVs to evaluate any issues.

2D ASIC: Dynamic Range



$$\text{Dynamic Range: } DR = \frac{\text{max charge}}{\text{min charge}} \approx \frac{Q_{\text{max}}}{3 ENC}$$

Given maximum input charge: $Q_{\text{max}} = 30 \text{ keV} = 8333 e^-$

and expected resolution: $ENC = 10 e^- \Rightarrow DR \approx 278$

2D ASIC: Dynamic Range => Power and Area

$$DR = \frac{\text{max charge}}{\text{min charge}} \approx \frac{Q_{\text{max}}}{3ENC} \approx \frac{C_S V_{S\text{max}} / G}{3\sqrt{ENC_{CA}^2 + 6kTC_S} / G^2}$$

After optimizing ENC_{CA} , designers set the charge gain **G so that** the contribution from the shaper **ENC_S** does not exceed **10 % of ENC_{CA}**

$$DR \approx \frac{C_S V_{S\text{max}}}{3\sqrt{10}\sqrt{6kTC_S}}$$

- To maximize the DR we need to use **rail-to-rail** configurations ($V_{S\text{max}} \rightarrow V_{DD}$)
- To maintain the same DR at lower V_{DD} we must **increase C_S** ($\downarrow V_{DD} \rightarrow \uparrow \uparrow C_S$)
- To increase C_S we must **increase Area and Power** of Shaper

$$\text{Area} [\mu\text{m}^2] \approx 10 \times 10^3 \times C_S [\text{pF}] \approx 0.023 \frac{DR^2}{V_{DD}^2}$$

↑
↑

high-order
 $\approx 1\text{fF}/\mu\text{m}^2$

$$\text{Power} [\mu\text{W}] \approx 4 \times V_{DD} C_S \frac{V_{DD}/10}{\tau_P/10} \approx 10^{-11} \frac{DR^2}{\tau_P}$$

↑
↑

high-order
slew rate

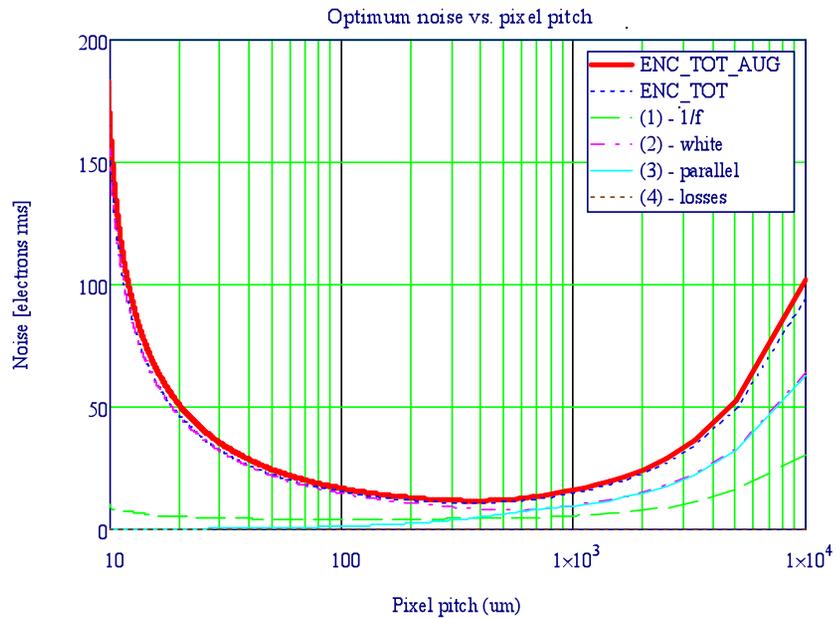
Given $DR \approx 278$, $V_{DD} = 3.3 \text{ V}$,
 $\tau_P = 1 \mu\text{s}$

☒ For Shaper:

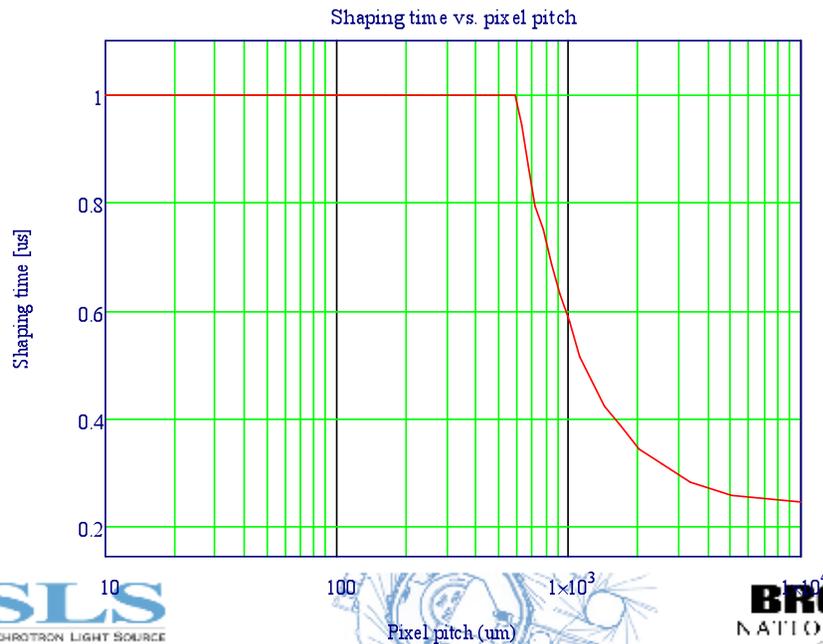
Area $\approx 163 \mu\text{m}^2$,

Power $\approx 0.77 \mu\text{W}$

2D ASIC: Detector Optimum Pixel Size for Noise



- shaping time < 1 μs
- shaper power: 0.77 μW
- spacing = pixel pitch / 6
- optimum pitch = 417 μm
- ENC_opt = 10.8 electrons rms



Collaborators

**G. De Geronimo, Shaorui Li, P. O'Connor, Z. Li, W. Chen, P. Rehak,
R. Beuttenmuller, D. Pinelli, J. Triolo, K. Wolniewicz,
A. Rumaiz, A. Kuczewski, R. Michta
D. Poshka, M. Pfeffer, J. Jakoncic**
*Brookhaven National Laboratory,
Upton, NY 11973, USA*

A. Dragone
SLAC, Stanford CA

H. F. Chuang
NSRRC, Taiwan

C. G. Ryan, G. Moorhead, R. Kirkham, P. Dunn
CSIRO, Clayton, Melbourne, Australia

G. Deptuch, M. Trimpl, R. Yarema, R. Lipton
Fermilab, Batavia, IL 60510

P. Grybos, P. Maj, R. Szczygiel
AGH UST, Krakow, Poland

Other BNL-related developments

Cryogenic detectors have recently begun to be applied to SR experiments.

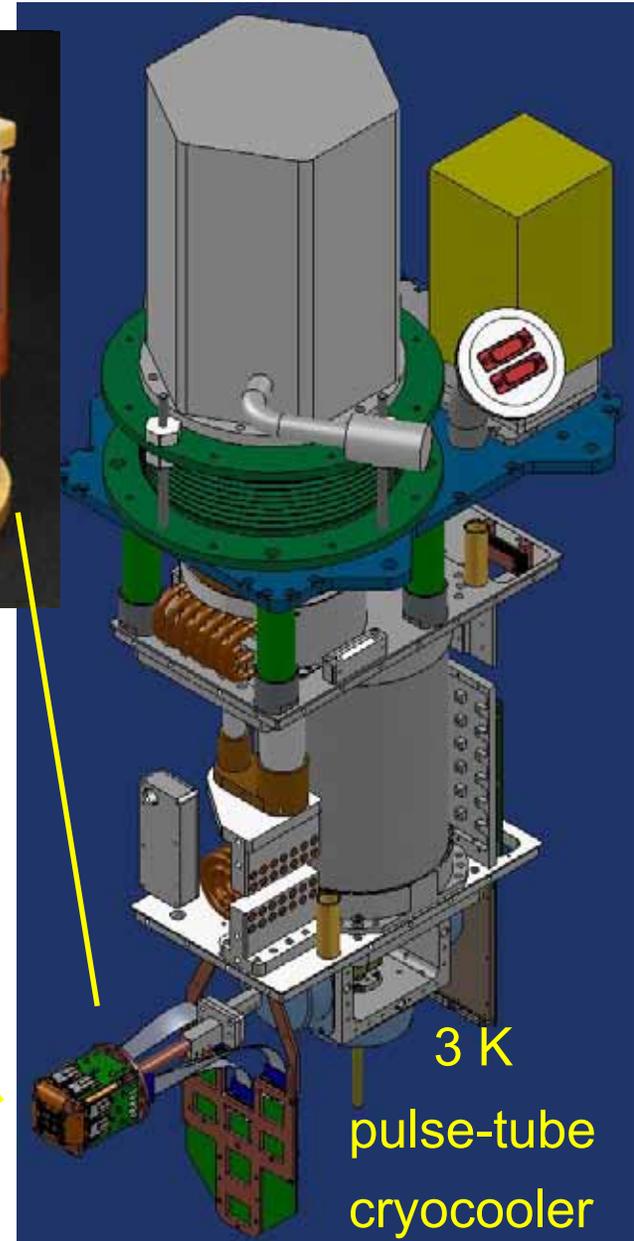
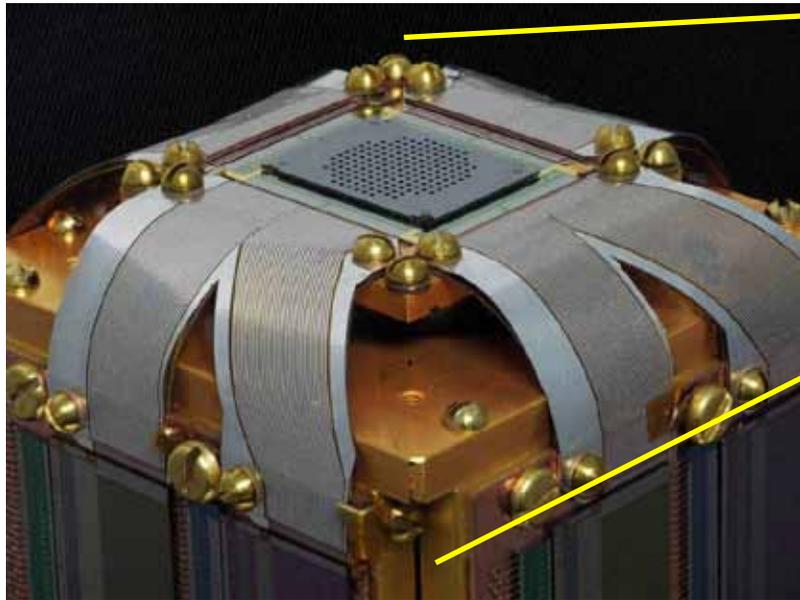
NIST Boulder is making a microcalorimeter array for use at NSLS beamline U7A.

W. Bertrand (Randy) Doriese (NIST Boulder)

Dan Fischer (NIST, NSLS beamline U7A
Spokesperson)



cal-XRF instrument for NSLS U7A



Target specs of instrument to be delivered in early 2011:

- 200 -1000 eV energy range
- 1 eV resolution
- 256 pixels
- 10 mm² total collecting area
- ~25 kHz total count rate

50 mK stage

3 K

pulse-tube cryocooler



Summary

- SR experiments are slowly learning to use modern detector technology.
- Funding agents are slowly realizing that new sensor technologies can provide improved performance.
- New sources raise new challenges for detector developers.
- 3D integration will certainly play a role in the future.