# FPGA PAD and Other Detector Developments at Cornell

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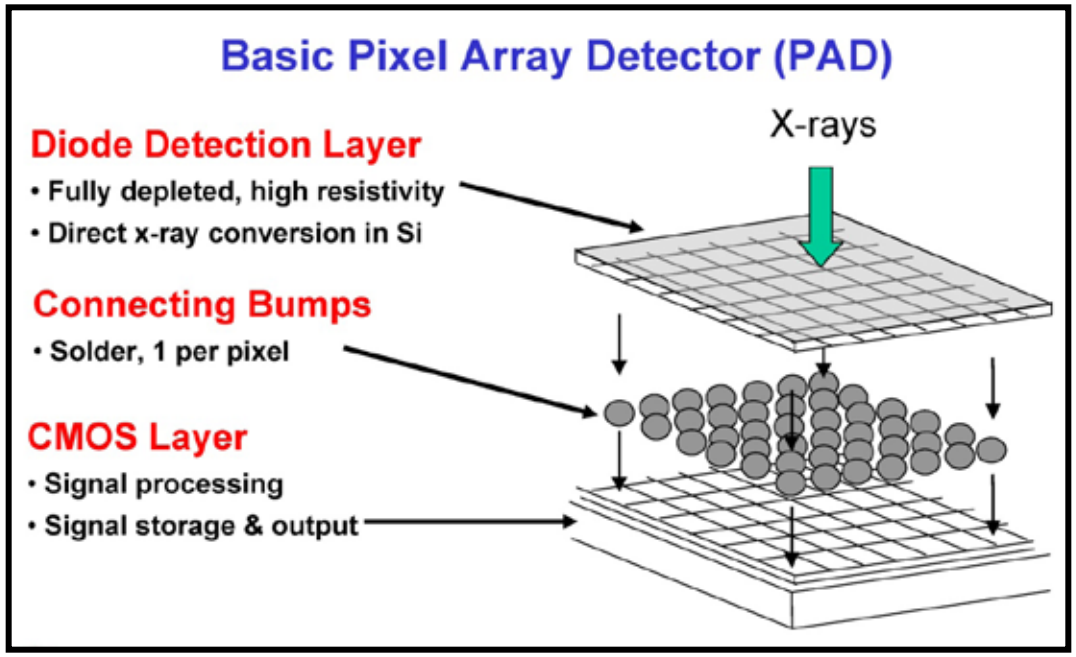
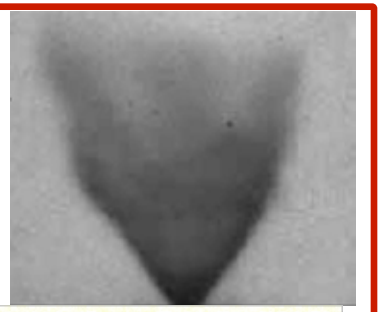
Sol Gruner: Context for this workshop talk.

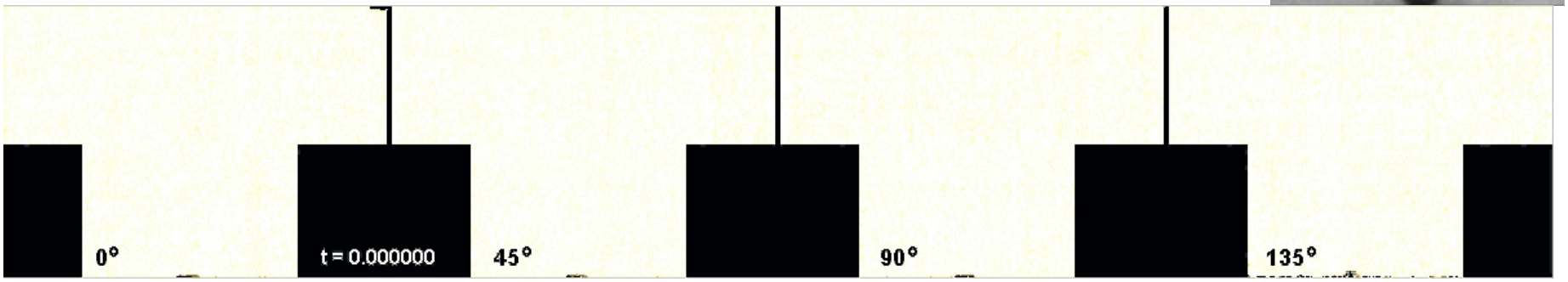
# Integrated Circuit technology now makes direct-detection semiconducto "Intelligent" Detector Feasible

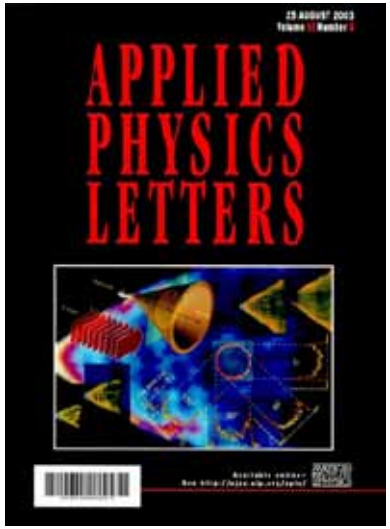
**An intelligent Pixel Array Detectors (PAD) has both advantages of direct detection and sophisticated data processing functions built into each pixel of the detector.**

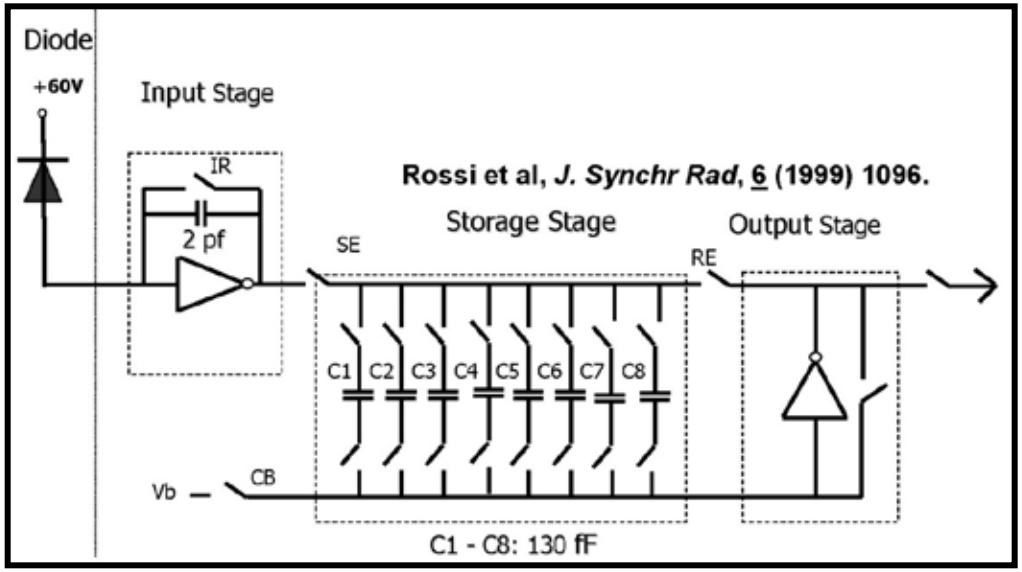


# Gasoline fuel injector spray

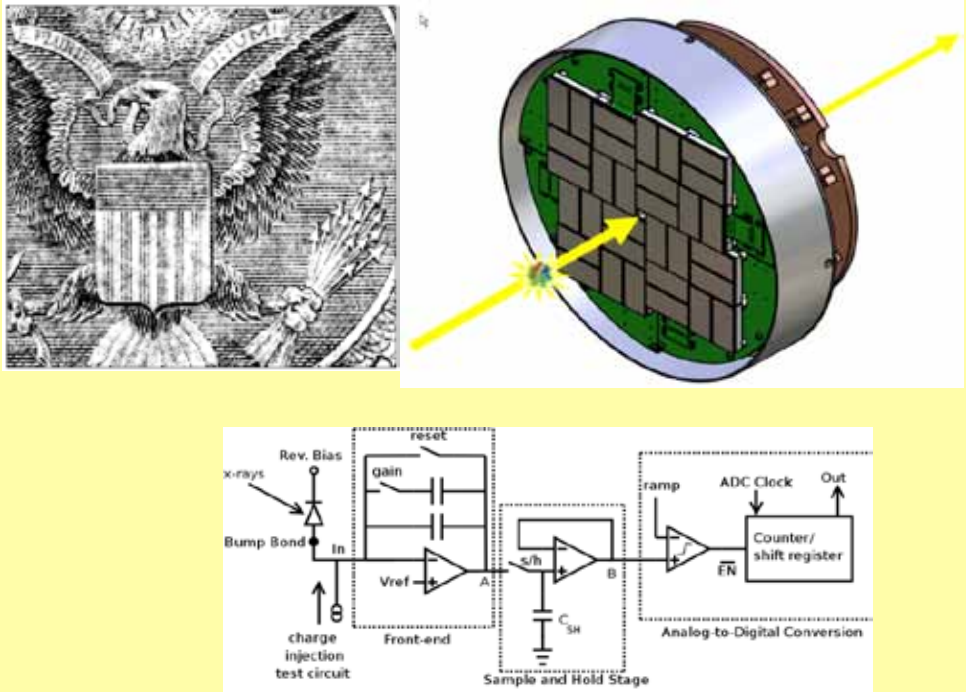





Collaboration with Jin Wang's group at APS. Recent work:
Liu *et al.*, Appl. Phys. Lett. **94** (2009) 184101

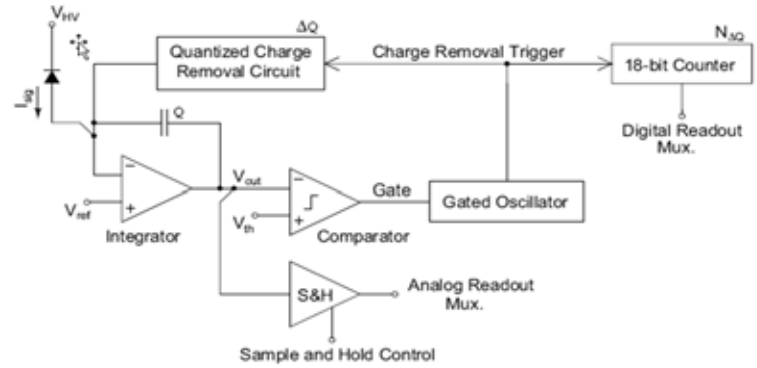


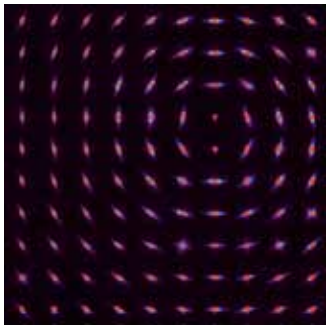

# LCLS PAD

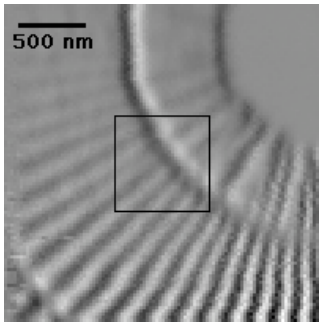
- Cornell role: Design PAD chips, build single chip, cooled detector to spec. Completed.
- SLAC role: Build mosaic & mechanicals, off-chip electronics. In process.
- Possible concerns: Warm operation affecting calibration stability and lifetime.
- More: Chris Kenney (this workshop), Hugh Philipp's plenary, Thursday morning.
- 0.5 GB/s, 50 TB/day, continuously!
- Papers: http://bigbro.biophys.cornell.edu/publications/ #225, 230, 243, 246

# Mixed-Mode PAD

| | |
|---|---|
| PAD Tile Format | 128 x 128 pixels |
| Pixel Size | 150 µm x 150 µm |
| Frame Rate | Up to 1,000 Hz |
| Read Noise | 0.3 X-ray [12 keV] / pix |
| Well Capacity | $2.6 \times 10^7$ X-ray [12 keV]/pix/frame |

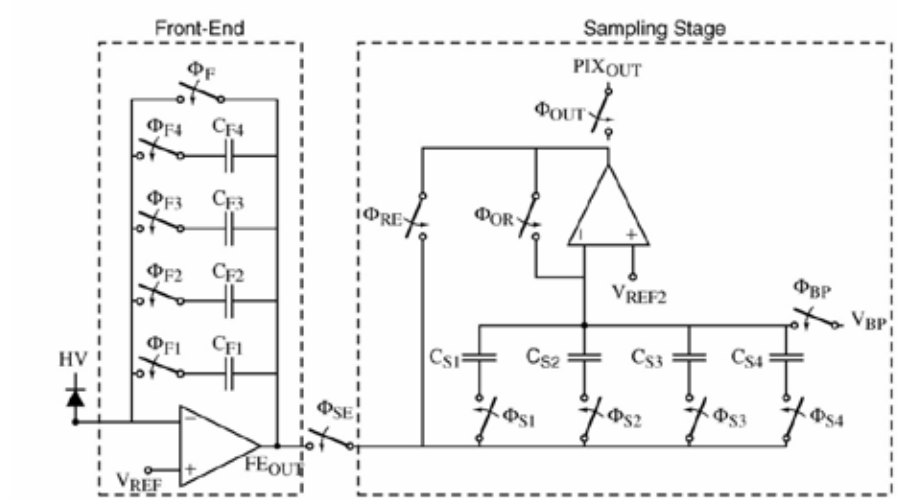


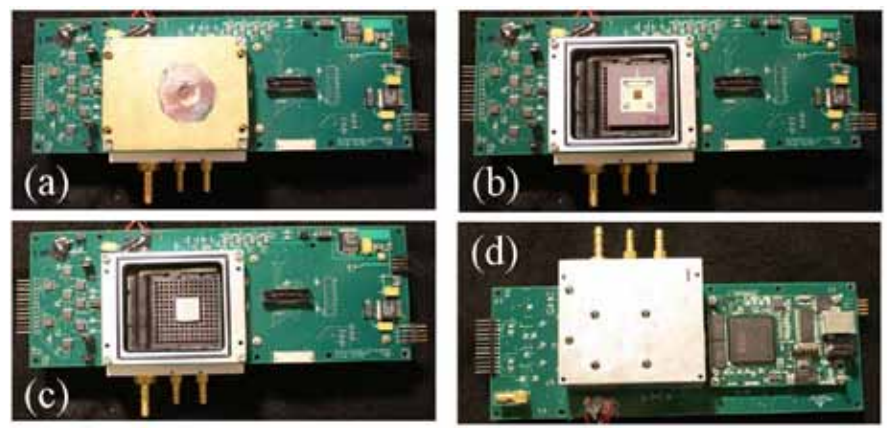






- Cornell role: Design PAD chips, build single chip, cooled detector to spec. Completed.
- ADSC role: Build large detectors & vend. In process.
- 65 MB/ASIC/s. For a 1k x 1k this is 400 TB/day, continuously!
- Papers: http://bigbro.biophys.cornell.edu/publications/ #196, 226, 25f

| KECK PAD | |
|---|---|
| **Parameter** | **Target Value** |
| Noise | < 0.5 x-ray/pixel/accumulation |
| Minimum exposure time | 150 ns for 8-bit imaging<br>1 µs for full-well imaging |
| Capacitor well depth | 2000 – 4000 x-rays |
| Nonlinearity (% full well) | < 0.2% |
| Diode conversion layer | 500 µm thick Si |
| Number of capacitor wells/pix | 5 – 8 |
| Full chip frame time | 10 msec/frame, e.g., 50 msec for 5 capacitors |
| Radiation lifetime | > 10 Mrad at detector face @ 8 keV |
| Pixel size | 150 µm on a side, or 128 x 128 pixels per IC |
| Detector chip format | 2 x 4 chips = 256 x 512 pixels |
| Dark current | 2 x-rays/pix/sec |




- **Designed for single bunch imaging at storage rings.**
- **Cornell role: Start to finish. Funded by Keck Foundation.**
- **Status: Pixel developed, 16x16 detector built and tested. Meets spec.**
- **Papers: http://bigbro.biophys.cornell.edu/publications/ #250.**
  **PhD thesis of Lucas Koerner, new paper is submitted.**

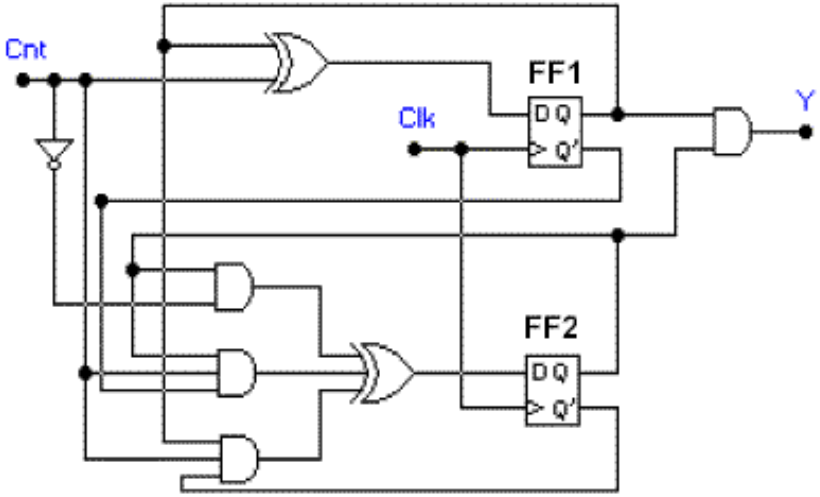
**The PAD development cycle is long, often 5-10 years.**

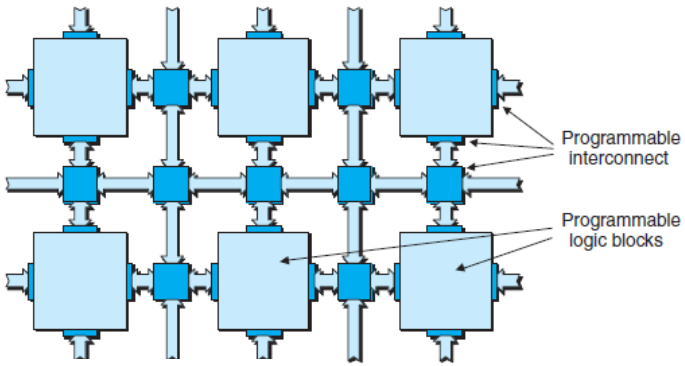
**What can we do to shorten the development time?**

# FPGA PAD

# What is an FPGA

- ***Field programmable gate arrays* a *(FPGAs) a*re digital integrated circuits (ICs) that:**
  - **contain configurable (programmable) blocks of logic**
  - **contain configurable interconnects between these blocks.**
  - **Design engineers can configure, or program "in the field" to perform a great variety of tasks**
  - **Are often able to be reprogrammed numerous times – SRAM based**
  - **Large numbers of input/output (I/O) pins for interfacing**
  - **Fast powerful massively parallel processing engine.**
  - **Contains internal ultra-fast RAM that can be distributed across an application**

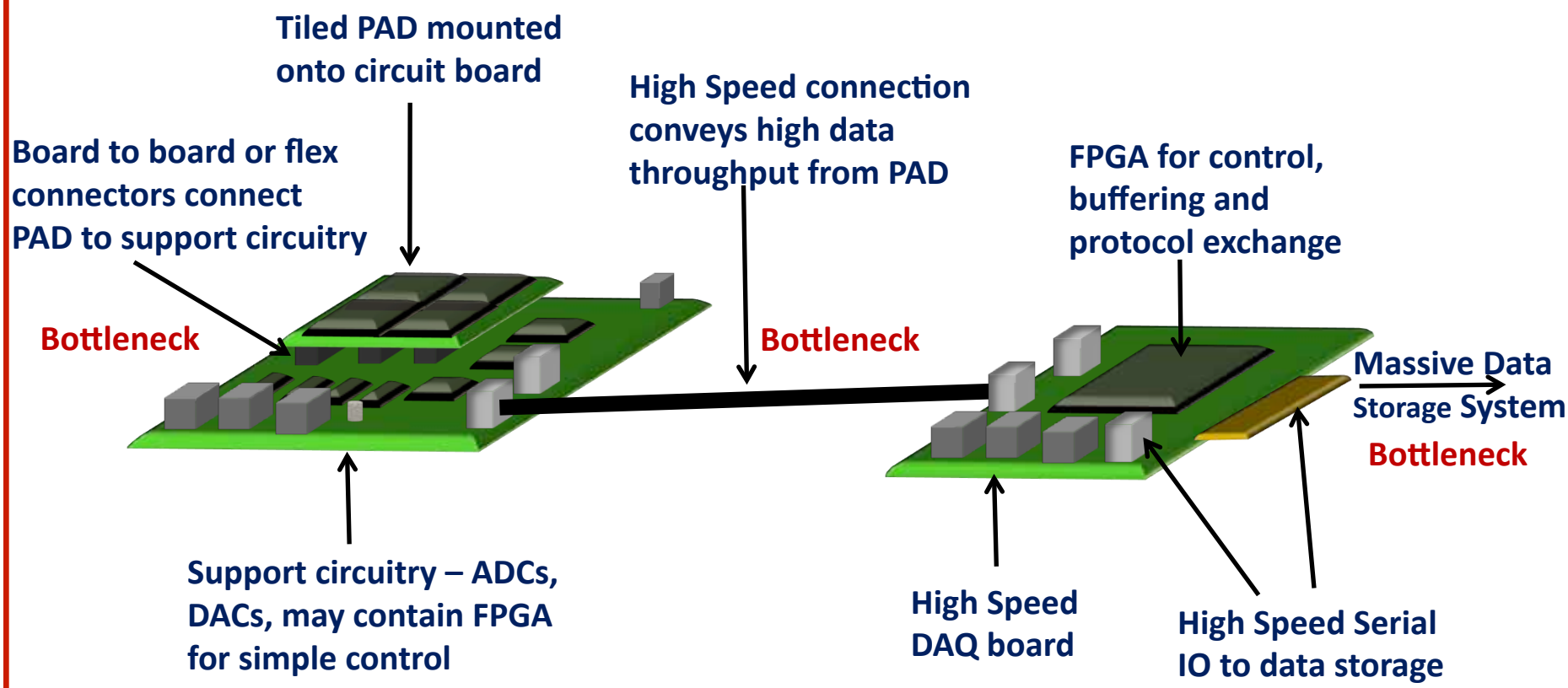


# FPGAs Processing Power over Time

| Device Family | Logic Cells | Maximum Block RAM | DSP slices | PCI Express interfaces | Maximum User IO | Ultra-fast IO |
|---|---|---|---|---|---|---|
| Virtex 4 | 142,00 | 6 Mbits | 512 | 0 | 960 | 24 |
| Virtex 5 | 330000 | 18 Mbits | 1056 | 4 (2 soft) | 1000 | 48 |
| Virtex 6 | 549,888 | 38 Mbits | 2000 | 4 | 1200 | 48 |
| Virtex 7 | 1,954,560 | 56 Mbits | 3900 | 4 | 1200 | 72 |

# Typical DAQ System for PADs



# Problems with current systems

- Most of the 'smarts' exist hardwired within the pixel
  - Tend to be application specific
  - Pixels may be large and complex
  - May contribute to lower yields
- Very high data transfer rates off the PAD
  - Often restrict maximum frame rate of PAD
  - Large number of high speed switching data lines susceptible to noise
- Huge amounts of data storage required
  - Most processing is done offline
  - FPGA is typically used as nothing more than a glorified buffer

# Proposed Architecture

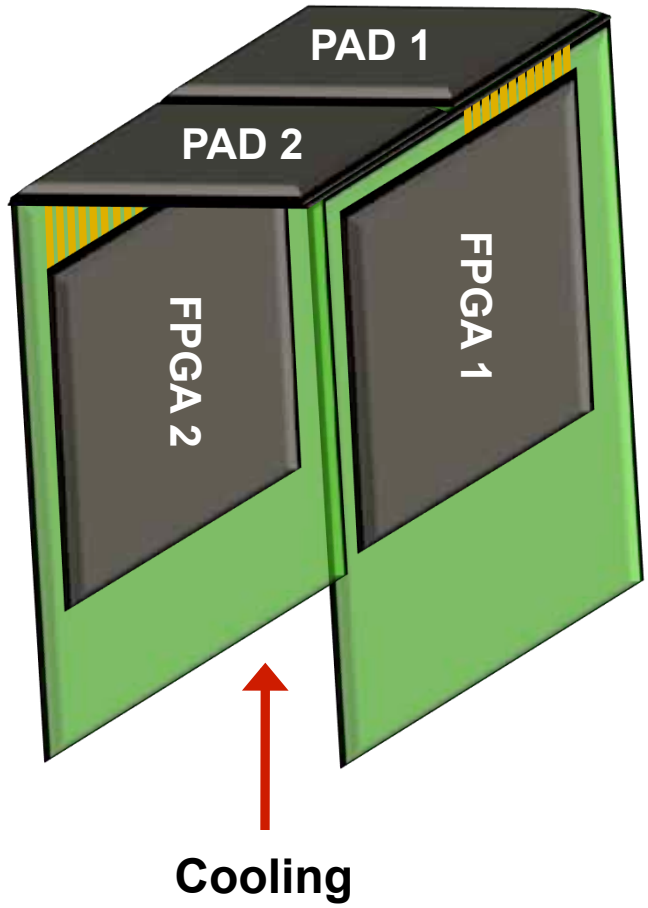
- **Close mating of CMOS ASIC and the FPGA so that the FPGA is an *integral resident part of the detector*, rather than just a part of the control hardware.**

- **Simple, fast pixels – essentially integrating front end and one-bit digitization**

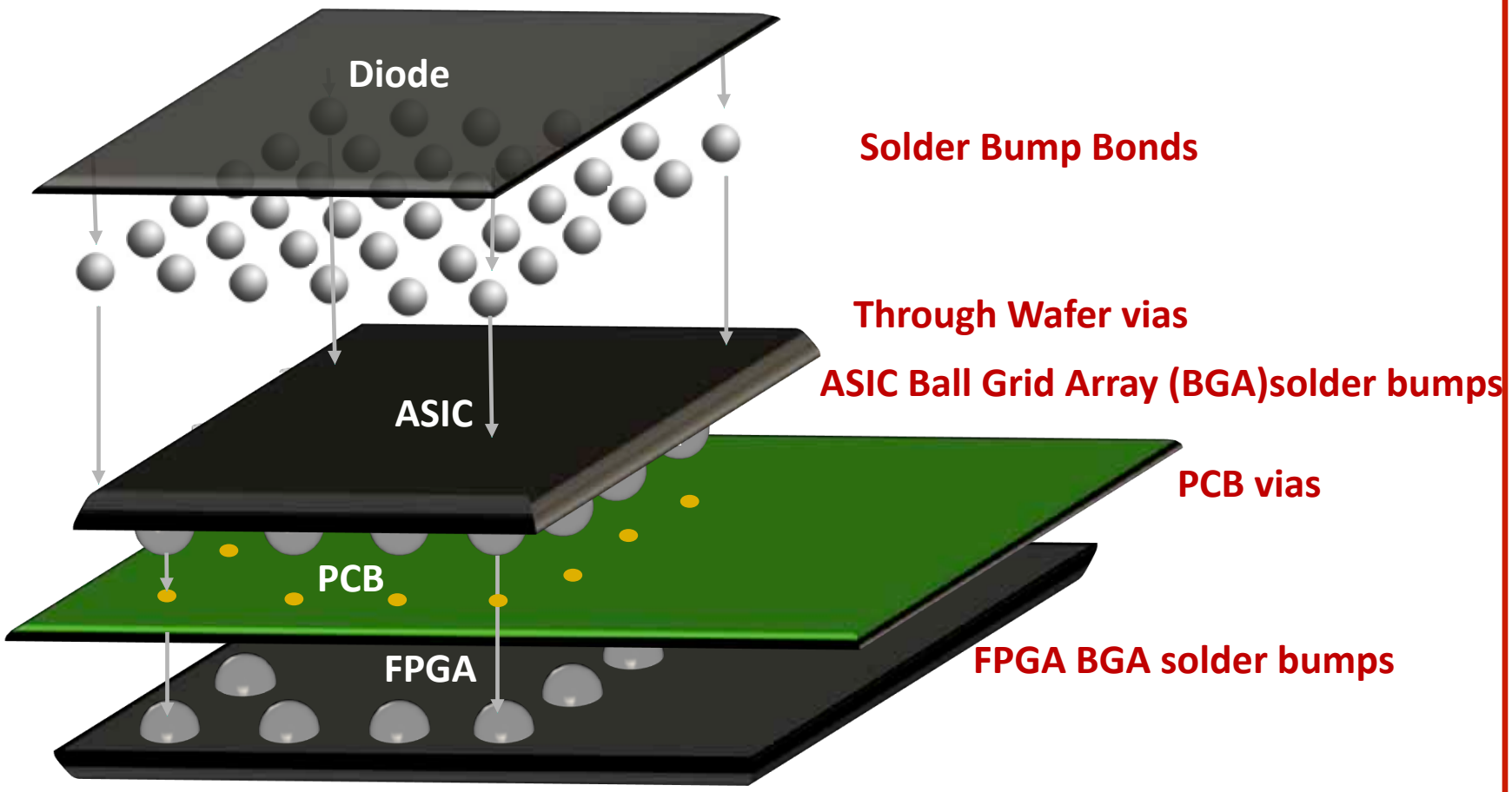
- **FPGA back-end whose reconfigurable implementation is tailored to meet various applications**

# FPGA PAD – One option

- FPGA 1 – massively parallel connection to PAD1
- FPGA 2– massively parallel connection to PAD2
- Advantages:
  - Tileable 2x1 unit
  - Can be cooled
- Disadvantages
  - Massively parallel connection between FPGA and PAD could be routing nightmare
  - At high switching speeds – skew, noise



# FPGA PAD – Another option (others are also being considered)



# Advantages of FPGA PAD Architecture

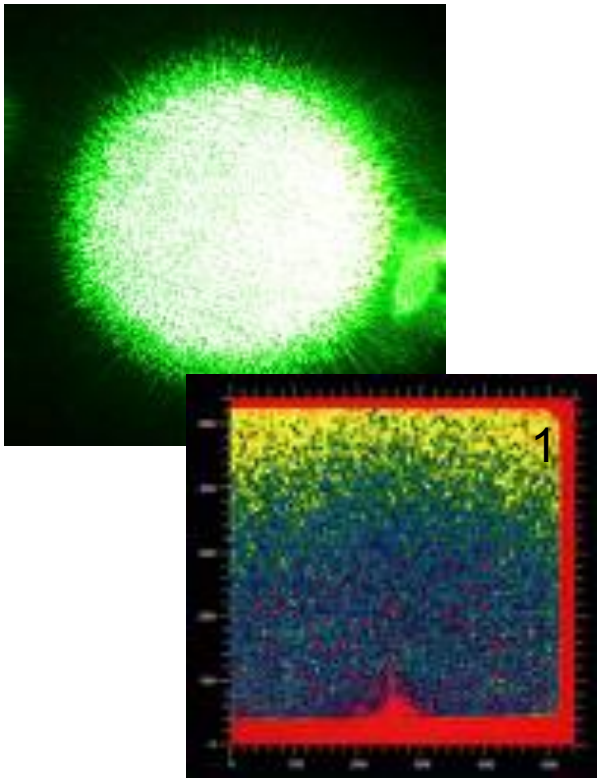
- The FPGA can be *re-programmed* to allow novel detectors to be tailored for different applications without changes to the ASIC.
- Processing of data can occur in *real time* reducing the actual data transferred to storage.

# Example Design

- **An example of a proposed design – an "in-pixel" autocorrelator for use in speckle measurements**

# Speckle Phenomena

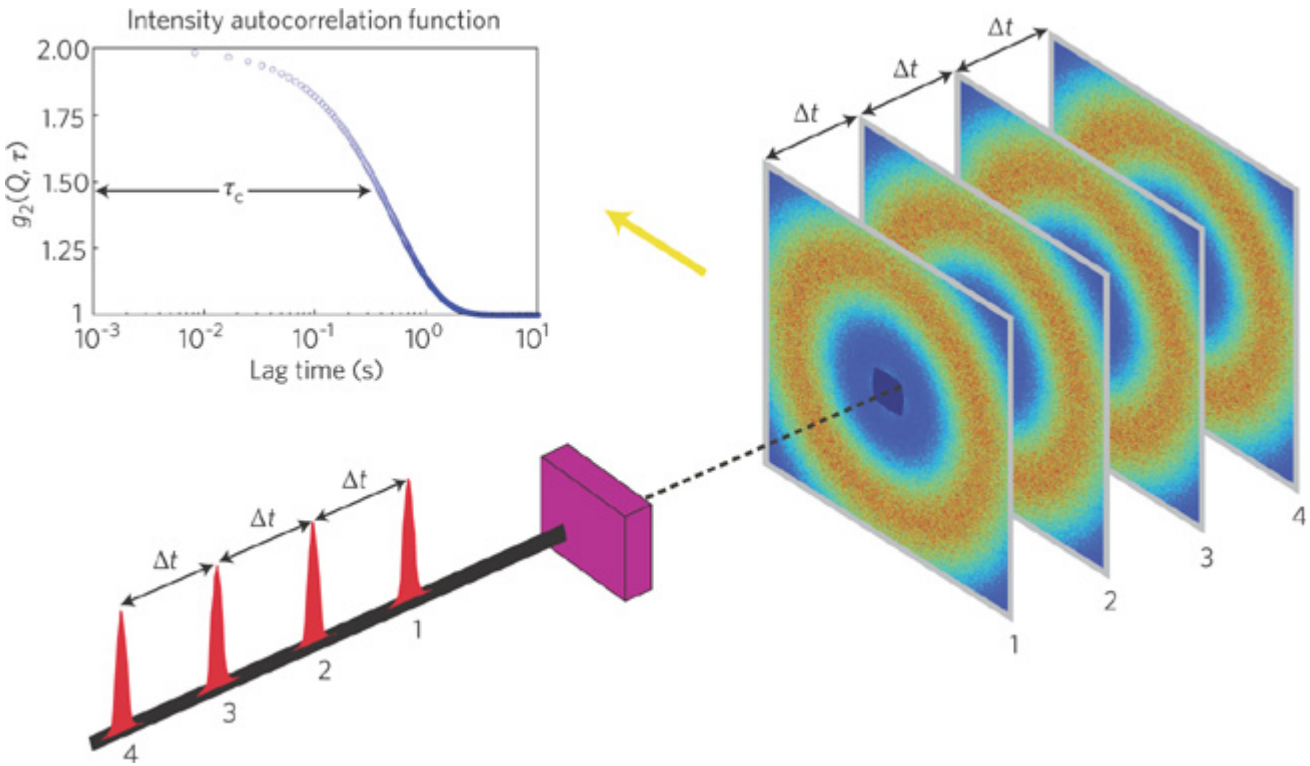
- *Speckle* - phenomena observed when a coherent photon source is scattered over a rough surface
- Each particle diffracts the wave separately each acting as a single point source
- These point sources interfere causing a 'speckle' pattern
- Speckle intensity variation over time observed due to dynamics such as Brownian motion
- Frequency of intensity variation related to natural movements within molecules
- X-Ray photon correlation spectroscopy (XPCS)is used to study these complex dynamics at the nm scale.
  - Intensity autocorrelation function performed on stored images to determine in-system dynamics




[1]Tsui, Mochrie, Berman, *J. Synchrotron Rad.* (1998). **5**, 30-36

# Intensity ACF in Speckle Measurements

Stephenson,.Robert,[2] Grübel,, *Nature Materials* **8**, 702 - 703 (2009)

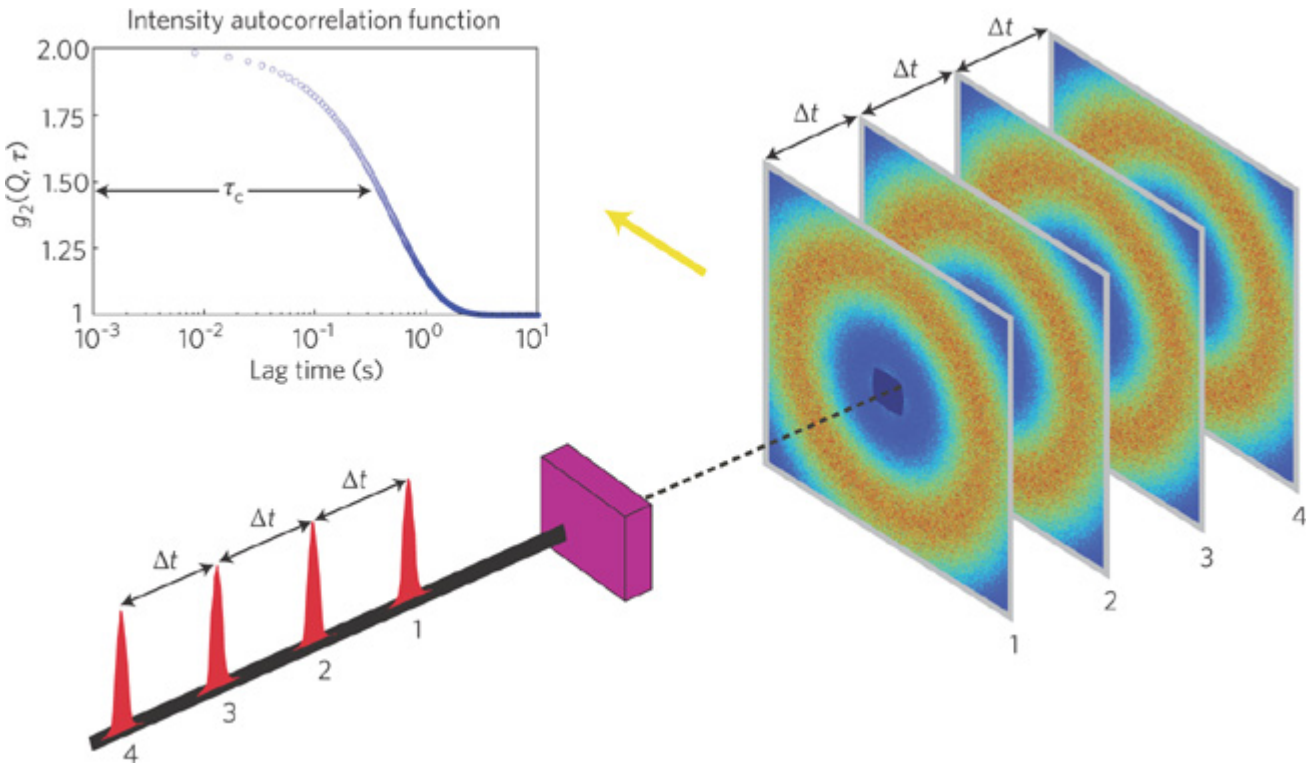



**Typically, a sequence of speckle patterns is recorded and the intensity autocorrelation function $g^2$ is used to determine a correlation time $\tau$ at each wavevector Q.**

$$g^2(q;\tau) = \frac{I(t)\cdot I(t+\tau)}{I(t)^2}$$

# Intensity ACF in Speckle Measurements

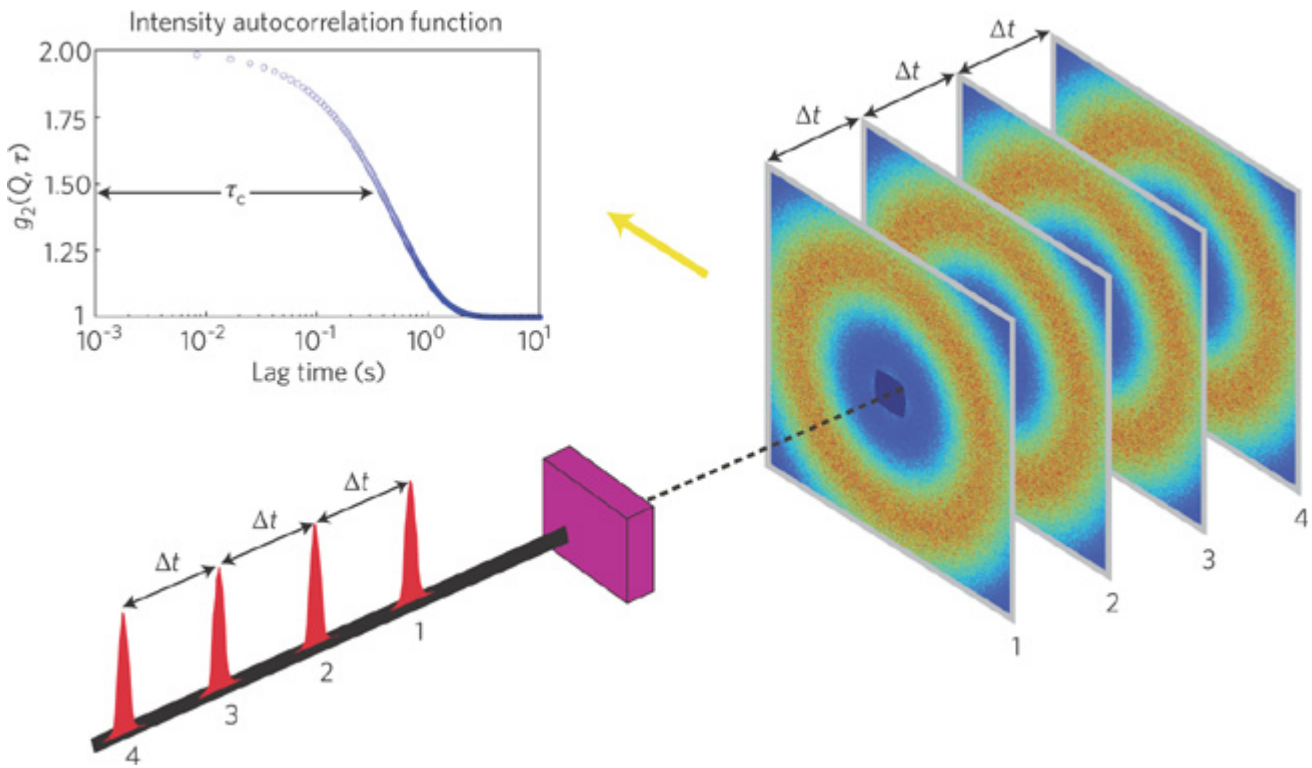
Stephenson,.Robert,[2] Grübel,, *Nature Materials* **8**, 702 - 703 (2009)




**The dynamics can be characterized on timescales as short as the time spacing *Δt* of the sequence.**

# Intensity ACF in Speckle Measurements

Stephenson,.Robert,[2] Grübel,, *Nature Materials* **8**, 702 - 703 (2009)



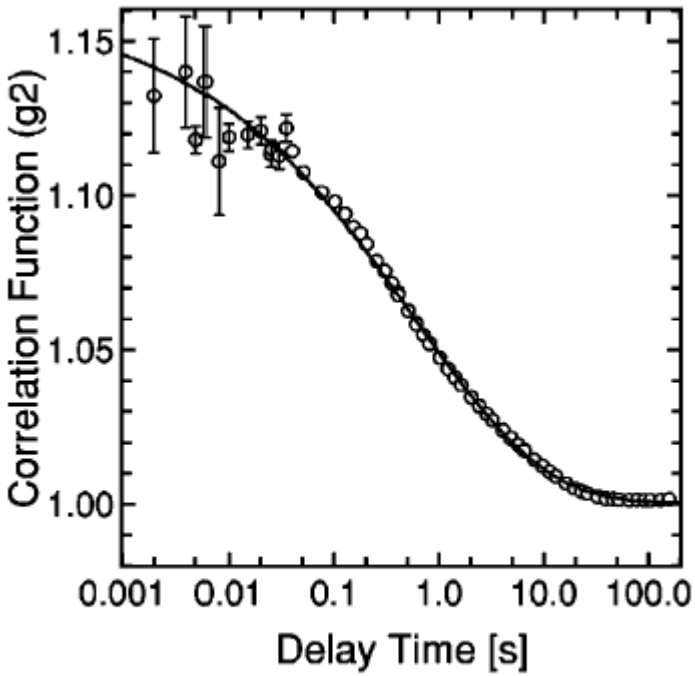

**To investigate times faster than the readout time of the detector, speckle patterns from two or more pulses can be summed and the decay in the contrast is used to determine the correlation times.**

# Why the FPGA PAD?

- At present minimum correlation time achievable is ~2 ms, limited by detector read-out time.
- FPGA PAD is designed to perform ACF at < 1us timescales
- Systems of interest with motions on sub-microsecond timescales include:
  - polymer creep
  - protein folding
  - phase transformations
  - …

# Why the FPGA PAD?

- CCD with $10^6$ pixels used as detector
- At least 120 frames to obtain figure
- 120 frames*$10^6$ pixels/frame*12 bits/pix= 144 Mb
- But how much data is in the plot?
  - 60 pts*12 bits/pt 720 bits
  - Off-detector reduction of x200,000
- If this calculation could be performed in real time…




Falus, Borthwick, Mochrie, RSI (2004) **75**, 4383-4400.

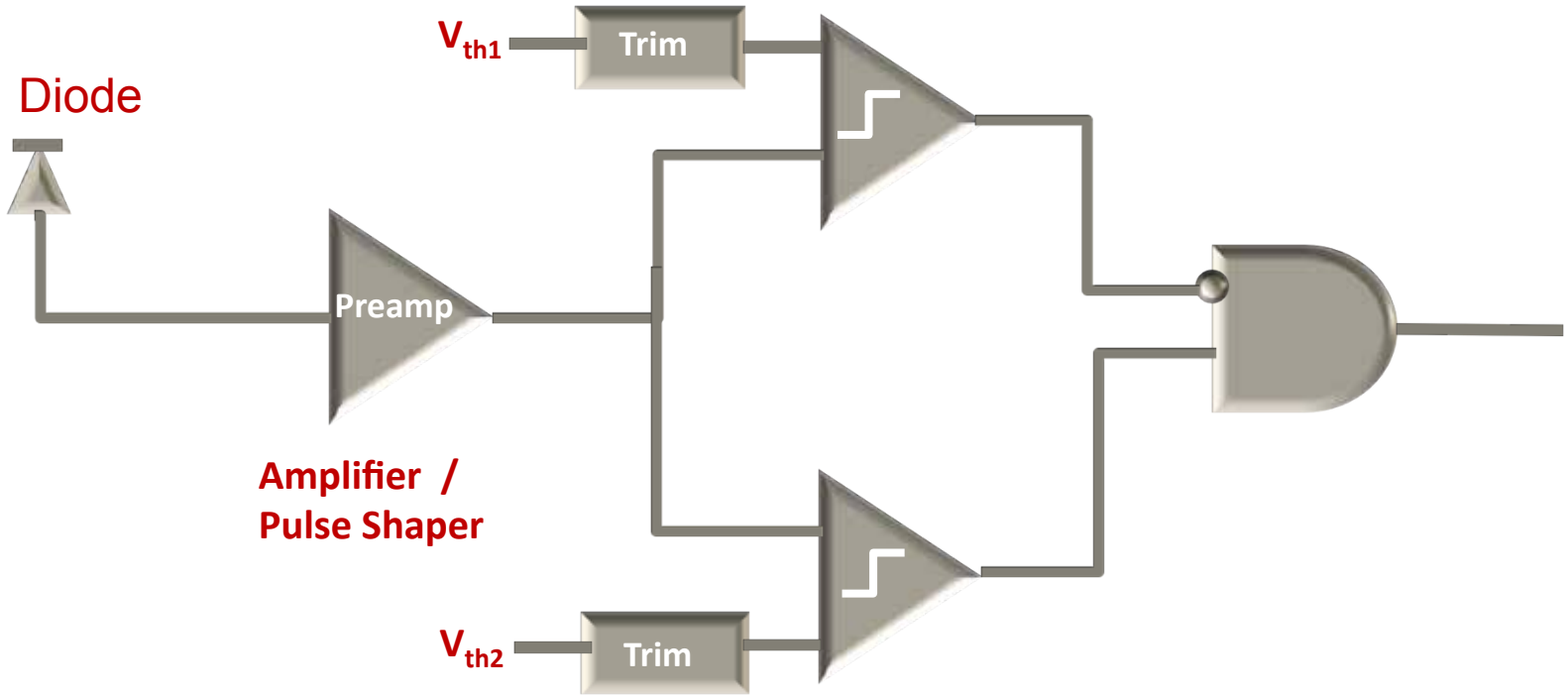
# Desired Specifications for FPGA PAD

- A relatively simple, small and fast pixel
- Massively parallel fast interconnect between the ASIC and the FPGA
- Parallel FPGA implementation of the Autocorrelation function to allow for correlations on sub-microsecond timescales
- Large reduction in data sent from the PAD to computer storage.

# Desired Specifications for FPGA PAD

| | |
|---|---|
| X-ray Count Rate | 1 MHz/ pixel |
| In-pixel shaping time | 100ns |
| Detector Layer | 300 – 500 µm Si |
| Energy Range | 4 – 15 keV |
| Number of Pixels | 10000 |
| Pixel size | 50 – 100 µm |
| Master Clock Speed | >150 MHz |
| Time autocorrelation function | 100 points , 1us to 10s |

# The Pixel – (One Option)

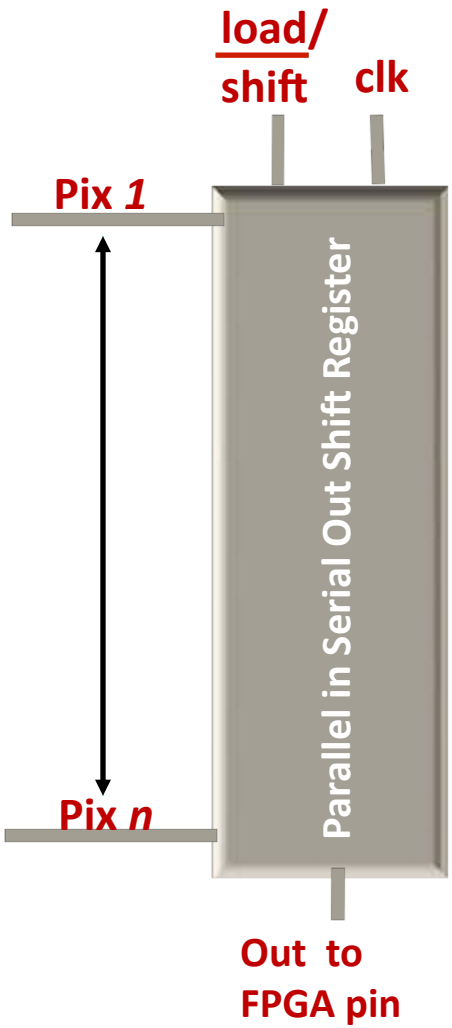



Energy Discriminator

# The Pixel Interface

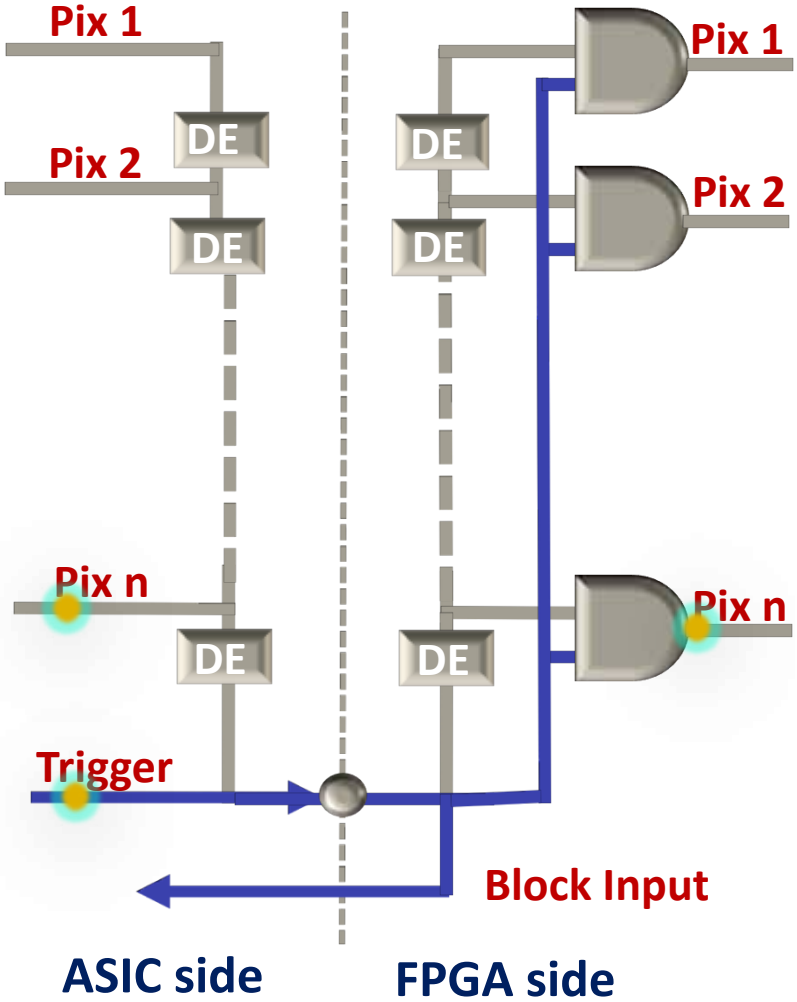
- The pixel pitch is much smaller than the pitch between FPGA pins. ( 100 µm to 1mm)
- Many pixels are ganged together into a group and fed through a single output pin of the ASIC into a single FPGA pin
  - In this initial design, 125 pixels/pin
- Two current ideas as to how this could be achieved:

# The Pixel Interface - Synchronous




- Pixels are polled at > 1 MHz to determine if an x-ray has passed through the single channel analyzer.
- The polling process is synchronous and controlled by a master clock from the FPGA.
- Polling speed restricted by maximum clock speed
  - Master FPGA clock to ASIC runs serious risk of skew at high clock speeds
  - Potential noise from switching clock
  - Local FPGA clock/group requires more pins

# The Pixel Interface - Asynchronous




- Trigger from ASIC informs FPGA group that an x-ray has been detected for one of the pixels in the group.
- Matched Delay Elements (DEs) between the ASIC and FPGA allow for each pixel to have a "time slot" to indicate its position
- Capable of much faster read-out speeds (DEs of <1ns possible)
- Low power
- Requires careful floor planning of delays on both FPGA and ASIC –
  - difficult routing
  - FPGA delay line must be matched to each ASIC
  - Requires very careful calibration

# FPGA Implementation of the ACF

- **At shorter time scales, the intensity levels become closer to a digital read of 1 or 0 x-rays recorded so the ACF:**

$$g^2(q;\tau) = \frac{I(t)\cdot I(t+\tau)}{I(t)^2}$$

- **Becomes**

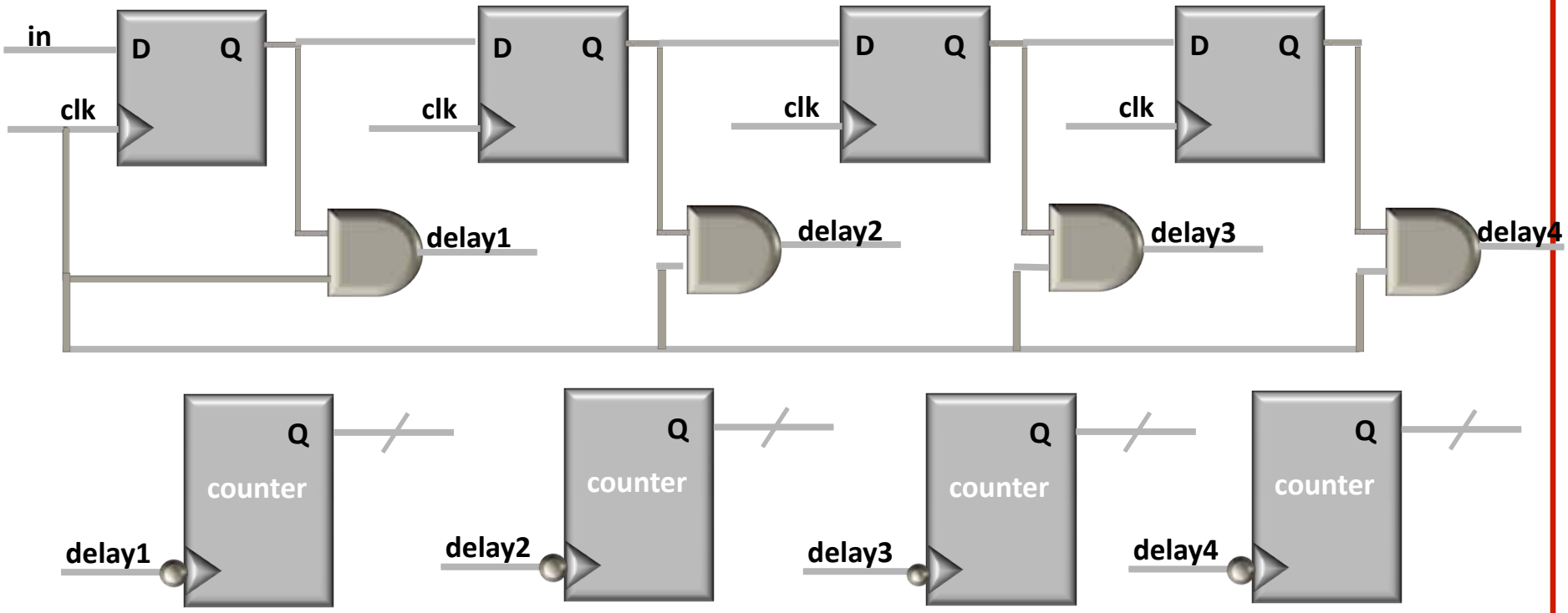
$$g^2(q;\tau) = I(t)\cdot I(t+\tau)$$

- **Which in discrete form is:**

$$g^2(q;j.\Delta t) = \sum_{i=1}^{N} X_i(t).X_i(t+j.\Delta t)$$

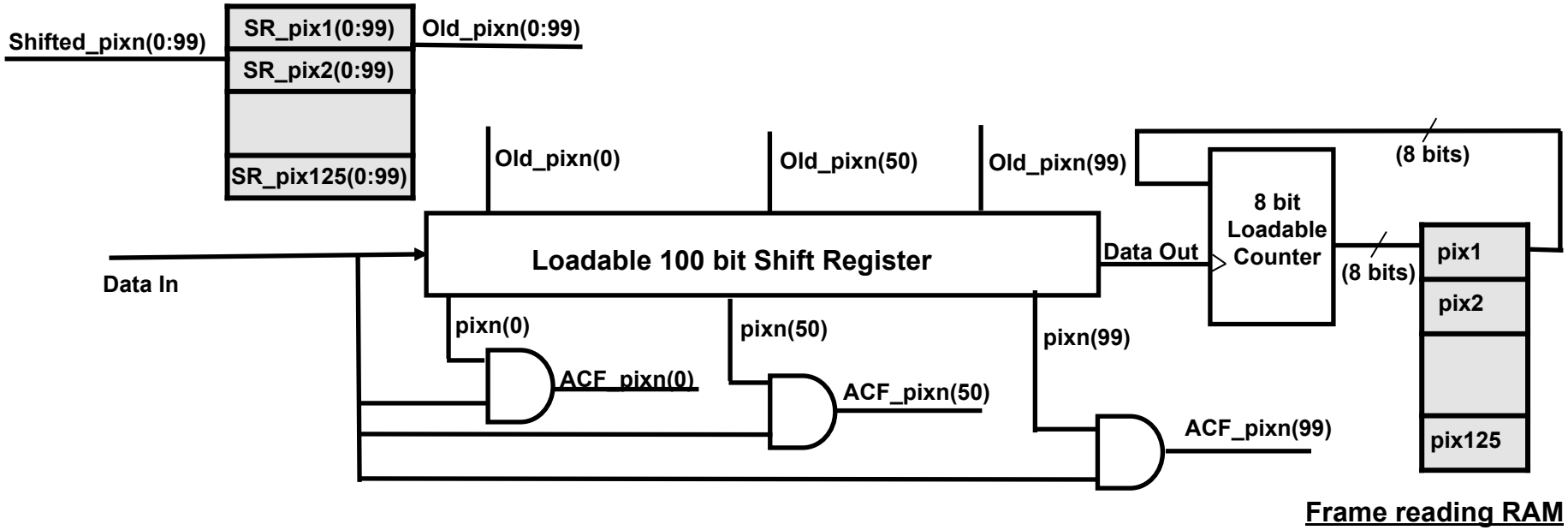
- **Where $X_i(t)$ takes on a 1 or 0 value dependant on the presence/absence of an x-ray on the detector during the time period.**
- **This is implemented using a sum of products method on an FPGA**

# FPGA Implementation of 4-point ACF




- The incoming pixel output is clocked in by the master clock and compared to its previous values over 4 different delays.
- Where there is coincidence (or correlation), the relevant counter is clocked. The outputs of these counters are the four ACF values

# Full Parallel FPGA ACF Implementation




- Not realizable to implement 100-bit shift register for each of the 125 pixels for each of the 100 input pins on the FPGA (over 10000 registers!!)

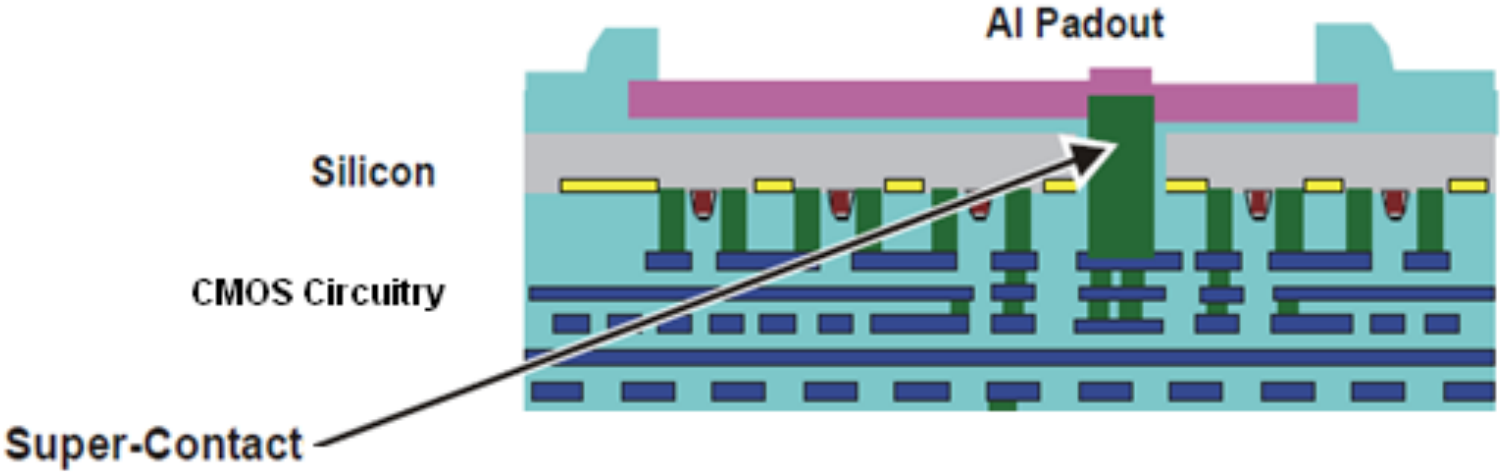
- 100-point shift register used for each pixel group and the ACF 'states' stored and retrieved from fast distributed RAM within the FPGA fabric.

# Physical Implementation of FPGA PAD

- In-house ASIC design – small scale submission in 2011
  - Test different possible pixels and interconnect mechanisms
- Through wafer via technology will be investigated at RTI during bump-bonding process
  - Use this to create BGA solder bump I/O from ASIC
  - Investigating the process to determine yield
- Xilinx Virtex7 FPGAs
  - offer large number of user IOs and large logic design area

# Through Silicon Interconnect Tezzaron Process

- Builds super-Contacts™ into the circuitry during normal wafer processing
- Back side of wafers thinned to < 10 microns exposing super-contacts
- Padded out for I/O



# Other potential applications of FPGA PAD by changing FPGA firmware

- **High Speed Imager**
  - As described, each pixel group is polled every 1us for a single bit readout.
  - Using an accumulator with RAM for every pixel group (FPGA input pin), 14 bits/pixel can be read out in 16ms for the PAD.
- **Time-sliced differencing detector**
  - Study metals that are subject to periodic stress, such as vibrations on an aircraft
  - Synchronize FPGA with the stress load so as to divide the stress cycle into time bins
  - Accumulate small differences between different cyclical time bins as a function of the number of cycles applied.

# Challenges

- **Design Challenges**
  - Maximizing speed of ASIC components – comparators, front-end amplifier, to maintain a fast front end
  - Design a pixel that is general enough to be ported across many applications (with a different FPGA backend)
  - Navigating the interconnection mechanism between the ASIC and FPGA for maximum throughput, low power consumption and low noise
  - If asynchronous option is investigated, matching delays for repeatability
  - …
- **Physical Challenges**
  - Making a modular detector for tiling – FPGA footprint much larger than the detector
  - Cooling the detector when it is in such close proximity to the high-speed switching FPGA
  - …

# Short Term Plans

- Still in pixel design stage. Hope for small scale submission in 2011 to test different prototype ideas
- Develop a test system (another FPGA) that can feed in signals mimicking the ASIC output so that the FPGA side of the interconnect can be tested
- Implement the massively ACF algorithm within the FPGA and optimize for speed.

# Acknowledgements


- **Cornell Detector Development Group**
  - Sol Gruner --- Mark Tate
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  - Darol Chamberlain --- Peiyan Cao
  - Marianne Hromalik --- Chen Shen
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  - Lucas Koerner (APL, Johns Hopkins) --- Matt Renzi (Lincoln Labs)
  - Daniel Schuette (Lincoln Labs) --- Alper Ercan
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  - National Science Foundation : NSF-DMR (DMR-0936384)
  - Department of Energy DOE-BES (DE-SC0004079) ,DOE-BER (DE-FG02-97ER62443) )
  - LCLSn Detector Group at SLAC
  - Area Detector Systems Corporation (ADSC)/NIH-NCRR
  - Keck Foundation